

Visvesvaraya Technological University, Belagavi Scheme of Teaching and Examinations-2022 Outcome-Based Education (OBE) and Choice Based Credit System (CBCS) (Effective from the academic year 2022-23)														
I Semester (Electrical & Electronics Engineering Stream)				(For Physics Group)										
Sl. No	Course and Course Code		Course Title	TD/PSB	Teaching Hours/Week				Examination				Credits	
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks		
														L
1	*ASC(IC)	BMATE101	Mathematics-I for EEE Streams	Maths	2	2	2	0	03	50	50	100	04	
2	#ASC(IC)	BPHYE102	Applied Physics for EEE Stream	PHY	2	2	2	0	03	50	50	100	04	
3	ESC	BEEE103	# Elements of Electrical Engineering	EEE/ECE/TCE					03	50	50	100	03	
		OR			2	2	0	0						
					OR									
		BBEE103	## Basic Electronics for EEE stream		3	0	0	0						
4	ESC-I	BESCK104x	Engineering Science Course-I	Respective Engg Dept	3	0	0	0	03	50	50	100	03	
5	ETC-I	BETCK105x	Emerging Technology Course-I	Any Dept	3	0	0	0	03	50	50	100	03	
	OR													
	PLC-I	BPLCK105x	Programming Language Course-I		2	0	2	0	03					
6	AEC	BENGK106	Communicative English	Humanities	1	0	0	0	01	50	50	100	01	
		OR												
		BPWSK106	Professional Writing Skills in English											
7	HSMC	BKSKK107/ BKBKK107	Sanskrutika Kannada/ Balake Kannada	Humanities	1	0	0	0	01	50	50	100	01	
		OR												
		BICOK107	Indian Constitution		1	0	0	0						
8	AEC/SDC	BIDTK158	Innovation and Design Thinking	Any Dept	1	0	0	0	01	50	50	100	01	
		OR												
		BSFHK158	Scientific Foundations of Health		1	0	0	0	01					

TOTAL										400	400	800	20
# Electrical & Electronics Engineering Students have to study BEEE103- Element of Electrical Engineering compulsorily ## Where as Electronics and allied stream students have to study BBEE103 Basic Electronics compulsorily													
SDA-Skill Development Activities, TD/PSB- Teaching Department / Paper Setting Board, ASC-Applied Science Course, ESC- Engineering Science Courses, ETC- Emerging Technology Course, AEC- Ability Enhancement Course, HSMS-Humanity and Social Science and Management Course, SDC- Skill Development Course, CIE-Continuous Internal Evaluation, SEE- Semester End Examination, IC – Integrated Course (Theory Course Integrated with Practical Course)													
Credit Definition: 1-hour Lecture (L) per week=1Credit 2-hoursTutorial(T) per week=1Credit 2-hours Practical / Drawing (P) per week=1Credit 2-hous Skill Development Actives (SDA) per week = 1 Credit							04-Credits courses are to be designed for 50 hours of Teaching-Learning Session 04-Credits (IC) are to be designed for 40 hours’ theory and 12-14 hours of practical sessions 03-Credits courses are to be designed for 40 hours of Teaching-Learning Session 02- Credits courses are to be designed for 25 hours of Teaching-Learning Session 01-Credit courses are to be designed for 12-15 hours of Teaching-Learning sessions						
Student’s Induction Program: Motivating (Inspiring) Activities under the Induction program – The main aim of the induction program is to provide newly admitted students a broad understanding of society, relationships, and values. Along with the knowledge and skill of his/her study, students’ character needs to be nurtured as an essential quality by which he/she would understand and fulfill the responsibility as an engineer. The following activities are to be covered in 21 days. Physical Activity, Creative Arts, Universal Human Values, Literary, Proficiency Modules, Lectures by Eminent People, Visits to Local areas, Familiarization with Department/Branch and Innovation, etc. For details, refer the ANNEXURE-I of Induction Programs notification of the University published at the beginning of the 1 st semester.													
AICTE Activity Points to be earned by students admitted to BE/ B.Tech., / B. Plan day college program (For more details refer to Chapter 6, AICTE Activity Point Program, Model Internship Guidelines): Over and above the academic grades, every regular student admitted to the 4 years Degree program and every student entering 4 years Degree programs through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE Activity Point Program. Students transferred from other Universities to the fifth semester are required to earn 50 Activity Points from the year of entry to VTU. The Activity Points earned shall be reflected on the student’s eighth semester Grade Card. The activities can be spread over the years, any time during the semester weekends, and holidays, as per the liking and convenience of the student from the year of entry to the program. However, the minimum hours requirement should be fulfilled. Activity Points (non-credit) do not affect SGPA/CGPA and shall not be considered for vertical progression. In case students fail to earn the prescribed activity Points, an Eighth Semester Grade Card shall be issued only after earning the required activity points. Students shall be admitted for the award of the degree only after the release of the Eighth semester Grade Card.													
*- BMATE101Shall have the 03 hours of theory examination(SEE), however, practical sessions question shall be included in the theory question papers. ** The mathematics subject should be taught by a single faculty member per division, with no sharing of the course(subject)module-wise by different faculty members. #- BPHYE102SEE shall have the 03 hours of theory examination and 02-03 hours of practical examination. ESC or ETC of 03 credits Courses shall have only a theory component (L:T :P:S=3:0:0:0) or if the nature the of course required experimental learning syllabus													

shall be designed as an Integrated course (L:T:P:S= 2:0:2:0),. **All 01 Credit-** courses shall have the SEE of 01 hours duration and the pattern of the question paper shall be MCQ

(ESC-I) Engineering Science Courses-I					(ETC-I) Emerging Technology Courses-I				
Code	Title	L	T	P	Code	Title	L	T	P
BESCK104A	Introduction to Civil Engineering	3	0	0	BETCK105A	Smart Materials and Systems	3	0	0
BESCK104B	Introduction to Electrical Engineering	3	0	0	BETCK105B	Green Buildings	3	0	0
BESCK104C	Introduction to Electronics Communication	3	0	0	BETCK105C	Introduction to Nano Technology	3	0	0
BESCK104D	Introduction to Mechanical Engineering	3	0	0	BETCK105D	Introduction to Sustainable Engineering	3	0	0
BESCK104E	Introduction to C Programming	2	0	2	BETCK105E	Renewable Energy Sources	3	0	0
					BETCK105F	Waste Management	3	0	0
					BETCK105G	Emerging Applications of Biosensors	3	0	0
					BETCK105H	Introduction to Internet of Things (IOT)	3	0	0
					BETCK105I	Introduction to Cyber Security	3	0	0
					BETCK105J	Introduction to Embedded System	3	0	0
(PLC-I) Programming Language Courses-I									
Code	Title	L	T	P					
BPLCK105A	Introduction to Web Programming	2	0	2					
BPLCK105B	Introduction to Python Programming	2	0	2					
BPLCK105C	Basics of JAVA programming	2	0	2					
BPLCK105D	Introduction to C++ Programming	2	0	2					
The course BESCK104E, Introduction to C Programming, and all courses under PLC and ETC groups can be taught by faculty of ANY DEPARTMENT									

- The student has to select one course from the ESC-I group.
- **EEE** Students shall opt for any one of the courses from the ESC-I group **except**, BESCK104B-**Introduction to Electrical Engineering** and **ECE/ETC/BM/ML** students shall opt any one of the courses from ESC-I **except** BESCK104C **Introduction to Electronics Engineering**
- The students have to opt for the courses from ESC group without repeating the course in either 1st or 2nd semester
- The students must select one course from either ETC-I or PLC-I group.
- If students study the subject from ETC-I in 1st semester he/she has to select the course from PLC-II in the 2nd semester and vice-versa

Visvesvaraya Technological University, Belagavi Scheme of Teaching and Examinations-2022 Outcome-Based Education (OBE) and Choice Based Credit System (CBCS) (Effective from the academic year 2022-23)													
II Semester (Electrical & Electronics Engineering Stream)				(For the students who attended 1 st semester under Physics Group)									
Sl. No	Course and Course Code		Course Title	TD/PSB	Teaching Hours/Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	*ASC(IC)	BMATE201	Mathematics-II for EESI	Maths	2	2	2	0	03	50	50	100	04
2	#ASC(IC)	BCHEE202	Chemistry for EES	Chemistry	2	2	2	0	03	50	50	100	04
3	ESC	BCEDK203	Computer-Aided Engineering Drawing	Civil/Mech Engg dept	2	0	2	0	03	50	50	100	03
4	ESC-II	BESCK204x	Engineering Science Course-II	Respective Engg Dept	3	0	0	0	03	50	50	100	03
5	PLC-II	BPLCK205x	Programming Language Course-II	Any Dept	2	0	2	0	03	50	50	100	03
	OR												
	ETC-II	BETCK205x	Emerging Technology Course-II		03	0	0	0	03				
6	AEC	BPWKS206	Professional Writing Skills in English	Humanities	1	0	0	0	01	50	50	100	01
			OR										
		BENGK206	Communicative English										
7	HSMS	BICOK207	Indian Constitution	Humanities	1	0	0	0	01	50	50	100	01
			OR										
		BKSKK207/ BKBKK207	Sanskritika Kannada/ Balake Kannada										
8	HSMS	BSFHK258	Scientific Foundations of Health	Any Dept.	1	0	0	0	01	50	50	100	01
			OR										
		BIDTK258	Innovation and Design Thinking		1	0	0	0	01				
TOTAL										400	400	800	20

29052023/V10 Scheme for EEE/ECE/ETC/EIE/BM/ML/IO

SDA-Skill Development Activities, **TD/PSB**- Teaching Department / Paper Setting Board, **ASC**-Applied Science Course, **ESC**- Engineering Science Courses, **ETC**- Emerging Technology Course, **AEC**- Ability Enhancement Course, **HSMS**-Humanity and Social Science and Management Course, **SDC**- Skill Development Course, **CIE** -Continuous Internal Evaluation, **SEE**- Semester End Examination, **IC** – Integrated Course (Theory Course Integrated with Practical Course)

*- BMATE201 Shall have the 03 hours of theory examination(SEE), however, practical sessions question shall be included in the theory question papers. ** **The mathematics subject should be taught by a single faculty member per division, with no sharing of the course(subject)module-wise by different faculty members.**

#- BCHEE202- SEE shall have the 03 hours of theory examination and 02-03 hours of practical examination

ESC or ETC of 03 credits Courses shall have only a theory component (L:T :P:S=3:0:0:0) or if the nature the of course required practical learning, syllabus shall be designed as an Integrated course (L:T:P:S= 2:0:2:0)

All 01 Credit- courses shall have the SEE of 01 hours duration and the pattern of the question paper shall be MCQ

(ESC-II) Engineering Science Courses-II					(ETC-II) Emerging Technology Courses-II				
Code	Title	L	T	P	Code	Title	L	T	P
BESCK201A	Introduction to Civil Engineering	3	0	0	BETCK205A	Smart materials and Systems	3	0	0
BESCK202B	Introduction to Electrical Engineering	3	0	0	BETCK205B	Green Buildings	3	0	0
BESCK203C	Introduction to Electronics Communication	3	0	0	BETCK205C	Introduction to Nano Technology	3	0	0
BESCK204D	Introduction to Mechanical Engineering	3	0	0	BETCK205D	Introduction to Sustainable Engineering	3	0	0
BESCK205E	Introduction to C Programming	2	0	2	BETCK205E	Renewable Energy Sources	3	0	0
					BETCK205F	Waste Management	3	0	0
					BETCK205G	Emerging Applications of Biosensors	3	0	0
					BETCK205H	Introduction to Internet of Things(IoT)	3	0	0
					BETCK205I	Introduction to Cyber Security	3	0	0
					BETCK205J	Introduction to Embedded System	3	0	0
(PLC-II) Programming Language Courses-II									
Code	Title	L	T	P					
BPLCK205A	Introduction to Web Programming	2	0	2					
BPLCK205B	Introduction to Python Programming	2	0	2					
BPLCK205C	Basics of JAVA programming	2	0	2					
BPLCK205D	Introduction to C++ Programming	2	0	2					
The course BESCK205E, Introduction to C Programming, and all courses under PLC and ETC groups can be taught by faculty of ANY DEPARTMENT									

- The student has to select one course from the ESC-II group.
- **EEE** Students shall opt for any one of the courses from the ESC-I group **except**, BESCK202-Introduction to Electrical Engineering and ECE/ETC/BM/ML students shall opt any one of the courses from ESC-I **except** BESCK203Introduction to Electronics Engineering
- The students have to opt for the courses from ESC group without repeating the course in either 1st or 2nd semester
- The students must select one course from either ETC-II or PLC-II group.
- If students study the subject from ETC-I in 1st semester he/she has to select the course from PLC-II in the 2nd semester and vice-versa

Visvesvaraya Technological University, Belagavi Scheme of Teaching and Examinations-2022 Outcome-Based Education (OBE) and Choice Based Credit System (CBCS) (Effective from the academic year 2022-23)													
I Semester (Electrical & Electronics Engineering Stream)					(For Chemistry Group)								
Sl. No	Course and Course Code		Course Title	TD/PSB	Teaching Hours/Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	*ASC(IC)	BMATE101	Mathematics-I for EES	Maths	2	2	2	0	03	50	50	100	04
2	#ASC(IC)	BCHEE102	Chemistry for EES	Chemistry	2	2	2	0	03	50	50	100	04
3	ESC	BCEDK103	Computer-Aided Engineering Drawing	Mechanical	2	0	2	0	03	50	50	100	03
4	ESC-I	BESCK104x	Engineering Science Course-I	Respective Engg Dept	3	0	0	0	03	50	50	100	03
5	ETC-I	BETCK105x	Emerging Technology Course-I	Any Dept	3	0	0	0	03	50	50	100	03
	OR												
	PLC-I	BPLCK105x	Programming Language Course-I		2	0	2	0	03				
6	AEC	BPWSK106	Professional Writing Skills in English	Humanities	1	0	0	0	01	50	50	100	01
			OR										
		BENGK106	Communicative English										
7	HSMS	BICOK107	Indian Constitution	Humanities	1	0	0	0	01	50	50	100	01
			OR										
		BKSKK107/ BKBKK107	Sanskritika Kannada/ Balake Kannada										
8	HSMS	BSFHK158	Scientific Foundations of Health	Any Dept.	1	0	0	0	01	50	50	100	01
			OR										
		BIDTK158	Innovation and Design Thinking		1	0	0	0	01				
TOTAL										400	400	800	20

SDA-Skill Development Activities, **TD/PSB**- Teaching Department / Paper Setting Board, **ASC**-Applied Science Course, **ESC**- Engineering Science Courses, **ETC**- Emerging Technology Course, **AEC**- Ability Enhancement Course, **HSMS**-Humanity and Social Science and Management Course, **SDC**- Skill Development Course, **CIE** -Continuous Internal Evaluation, **SEE**- Semester End Examination, **IC** – Integrated Course (Theory Course Integrated with Practical Course)

*- BMATE101 Shall have the 03 hours of theory examination (SEE), however, practical sessions question shall be included in the theory question papers. ** **The mathematics subject should be taught by a single faculty member per division, with no sharing of the course(subject)module-wise by different faculty members.**

#- BCHEE102- SEE shall have the 03 hours of theory examination and 02-03 hours of practical examination

ESC or ETC of 03 credits Courses shall have only a theory component (L:T :P:S=3:0:0:0) or if the nature the of course required practical learning syllabus shall be designed as an Integrated course (L:T:P:S= 2:0:2:0) **All 01 Credit-** courses shall have the SEE of 01 hours duration and the pattern of the question paper shall be MCQ

Credit Definition:

1-hour Lecture (**L**) per week=**1Credit**

2-hours Tutorial(**T**) per week=**1Credit**

2-hours Practical / Drawing (**P**) per week=**1Credit**

2-hous Skill Development Actives (**SDA**) per week = **1 Credit**

04-Credits courses are to be designed for 50 hours of Teaching-Learning Session

04-Credits (IC) are to be designed for 40 hours' theory and 12-14 hours of practical sessions

03-Credits courses are to be designed for 40 hours of Teaching-Learning Session

02- Credits courses are to be designed for 25 hours of Teaching-Learning Session

01-Credit courses are to be designed for 12-15 hours of Teaching-Learning sessions

Student's Induction Program: Motivating (Inspiring) Activities under the Induction program – The main aim of the induction program is to provide newly admitted students a broad understanding of society, relationships, and values. Along with the knowledge and skill of his/her study, students' character needs to be nurtured as an essential quality by which he/she would understand and fulfill the responsibility as an engineer. The following activities are to be covered in 21 days. Physical Activity, Creative Arts, Universal Human Values, Literary, Proficiency Modules, Lectures by Eminent People, Visits to Local areas, Familiarization with Department/Branch and Innovation, etc. For details, refer the ANNEXURE-I of Induction Programs notification of the University published at the beginning of the 1st semester.

AICTE Activity Points to be earned by students admitted to BE/ B.Tech., / B. Plan day college program (For more details refer to Chapter 6, AICTE Activity Point Program, Model Internship Guidelines): Over and above the academic grades, every regular student admitted to the 4 years Degree program and every student entering 4 years Degree programs through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE Activity Point Program. Students transferred from other Universities to the fifth semester are required to earn 50 Activity Points from the year of entry to VTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card. The activities can be spread over the years, any time during the semester weekends, and holidays, as per the liking and convenience of the student from the year of entry to the program. However, the minimum hours' requirement should be fulfilled. Activity Points (non-credit) do not affect SGPA/CGPA and shall not be considered for vertical progression. In case students fail to earn the prescribed activity Points, an Eighth Semester Grade Card shall be issued only after earning the required activity points. Students shall be admitted for the award of the degree only after the release of the Eighth semester Grade Card.

(ESC-I) Engineering Science Courses-I					(ETC-I) Emerging Technology Courses-I				
Code	Title	L	T	P	Code	Title	L	T	P
BESCK104A	Introduction to Civil Engineering	3	0	0	BETCK105A	Smart Materials and Systems	3	0	0
BESCK104B	Introduction to Electrical Engineering	3	0	0	BETCK105B	Green Buildings	3	0	0
BESCK104C	Introduction to Electronics Communication	3	0	0	BETCK105C	Introduction to Nano Technology	3	0	0
BESCK104D	Introduction to Mechanical Engineering	3	0	0	BETCK105D	Introduction to Sustainable Engineering	3	0	0
BESCK104E	Introduction to C Programming	2	0	2	BETCK105E	Renewable Energy Sources	3	0	0
					BETCK105F	Waste Management	3	0	0
					BETCK105G	Emerging Applications of Biosensors	3	0	0
					BETCK105H	Introduction to Internet of Things (IOT)	3	0	0
					BETCK105I	Introduction to Cyber Security	3	0	0
					BETCK105J	Introduction to Embedded System	3	0	0
(PLC-I) Programming Language Courses-I									
Code	Title	L	T	P					
BPLCK105A	Introduction to Web Programming	2	0	2					
BPLCK105B	Introduction to Python Programming	2	0	2					
BPLCK105C	Basics of JAVA programming	2	0	2					
BPLCK105D	Introduction to C++ Programming	2	0	2					
The course BESCK104E Introduction to C Programming, and all courses under PLC and ETC groups can be taught by faculty of ANY DEPARTMENT									

- The student has to select one course from the ESC-I group.
- **EEE** Students shall opt for any one of the courses from the ESC-I group **except**, BESCK104B-**Introduction to Electrical Engineering and ECE/ETC/BM/ML** students shall opt any one of the courses from ESC-I **except** BESCK104C **Introduction to Electronics Engineering**
- The students have to opt for the courses from ESC group without repeating the course in either 1st or 2nd semester
- The students must select one course from either ETC-I or PLC-I group.
- If students study the subject from ETC-I in 1st semester he/she has to select the course from PLC-II in the 2nd semester and vice-versa

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Sl. No	Course and Course Code		Course Title	TD /PSB	Teaching Hours/Week				Examination				Credits
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2	#ASC(IC)	BPHYE202	Applied Physics for EES	PHY	2	2	2	0	03	50	50	100	04
3	ESC	BEEE203	# Elements of Electrical Engineering	EEE/ECE/TCE					03	50	50	100	03
		2 2 0 0											
		OR											
		BBEE203	## Basic Electronics			3	0	0					
4	ESC-II	BESCK204x	Engineering Science Course-II	Respective Engg Dept.	3	0	0	0	03	50	50	100	03
5	PLC-II	BPLCK205x	Programming language Course-II	Any Dept	2	0	2	0	03	50	50	100	03
	OR												
	ETC-II	BETCK205x	Emerging Technology Course-II		3	0	0	0	03				
6	AEC	BENGK206	Communicative English	Humanities	1	0	0	0	01	50	50	100	01
		OR											
		BPWSK206	Professional Writing Skills in English										
7	HSMC	BKSKK207/ BKBKK207	Sanskritika Kannada/ Balake Kannada	Humanities	1	0	0	0	01	50	50	100	01
		OR											
		BICOK207	Indian Constitution		1	0	0	0					
8	AEC/SDC	BIDTK258	Innovation and Design Thinking	Any Dept	1	0	0	0	01	50	50	100	01
		OR											
		BSFHK258	Scientific Foundations of Health		1	0	0	0	01				
TOTAL										400	400	800	20

Electrical & Electronics Engineering Students have to study BEEE203 Elements of Electrical Engineering compulsorily ## Whereas Electronics and allied stream students have to study BBEE203 Basic Electronics compulsorily
SDA-Skill Development Activities, TD/PSB- Teaching Department / Paper Setting Board, ASC-Applied Science Course, ESC- Engineering Science Courses, ETC- Emerging Technology Course, AEC- Ability Enhancement Course, HSMS-Humanity and Social Science and Management Course, SDC- Skill Development Course, CIE-Continuous Internal Evaluation, SEE- Semester End Examination, IC – Integrated Course (Theory Course Integrated with Practical Course)
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(ESC-II) Engineering Science Courses-II					(ETC-II) Emerging Technology Courses-II				
Code	Title	L	T	P	Code	Title	L	T	P
BESCK204A	Introduction to Civil Engineering	3	0	0	BETCK205A	Smart materials and Systems	3	0	0
BESCK204B	Introduction to Electrical Engineering	3	0	0	BETCK205B	Green Buildings	3	0	0
BESCK204C	Introduction to Electronics Communication	3	0	0	BETCK205C	Introduction to Nano Technology	3	0	0
BESCK204D	Introduction to Mechanical Engineering	3	0	0	BETCK205D	Introduction to Sustainable Engineering	3	0	0
BESCK204E	Introduction to C Programming	2	0	2	BETCK205E	Renewable Energy Sources	3	0	0
					BETCK205F	Waste Management	3	0	0
					BETCK205G	Emerging Applications of Biosensors	3	0	0
					BETCK205H	Introduction to Internet of Things(IoT)	3	0	0
					BETCK205I	Introduction to Cyber Security	3	0	0
					BETCK205J	Introduction to Embedded System	3	0	0
(PLC-II) Programming Language Courses-II									
Code	Title	L	T	P					
BPLCK205A	Introduction to Web Programming	2	0	2					
BPLCK205B	Introduction to Python Programming	2	0	2					
BPLCK205C	Basics of JAVA programming	2	0	2					
BPLCK205D	Introduction to C++ Programming	2	0	2					
The course BESCK204E, Introduction to C Programming, and all courses under PLC and ETC groups can be taught by faculty of ANY DEPARTMENT									

- The student has to select one course from the ESC-II group.
- **EEE** Students shall opt for any one of the courses from the ESC-I group **except**, BESCK204B-**Introduction to Electrical Engineering and ECE/ETC/BM/ML** students shall opt any one of the courses from ESC-I **except** BESCK204C **Introduction to Electronics Engineering**
- The students have to opt for the courses from ESC group without repeating the course in either 1st or 2nd semester
- The students must select one course from either ETC-II or PLC-II group.
- If students study the subject from ETC-I in 1st semester he/she has to select the course from PLC-II in the 2nd semester and vice-versa

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.Tech.in Electronics and Computer Engineering**Scheme of Teaching and Examinations 2022**

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2023-24)

III SEMESTER													
Sl. No	Course	Course Code	Course Title	Teaching Department (TD) and Question and Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEEMarks	Total Marks	
					L	T	P	S					
1	PCC	BMATELCE301	Mathematics for Electronics and Computers	TD: Maths PSB: Maths	3	0	0		03	50	50	100	3
2	IPCC	BUE302	Data Structures with C	TD:ECE/CSE PSB:ECE/CSE	3	0	2		03	50	50	100	4
3	IPCC	BUE303	Analog and Digital Electronics	TD:ECE PSB:ECE	3	0	2		03	50	50	100	4
4	PCC	BUE304	Microcontroller and Computer	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
5	PCCL	BUEL305	Python Programming Laboratory	TD:ECE/CSE PSB:ECE/CSE	0	0	2		03	50	50	100	1
6	ESC	BUE306x	ESC/ETC/PLC	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
7	UHV	BSCK307	Social Connect and	Any Department	0	0	2		01	100	---	100	1
8	AEC/ SEC	BUE358x	Ability Enhancement Course/Skill Enhancement Course - III		If the course is a Theory				01	50	50	100	1
					1	0	0						
					If a course is a laboratory				02				
					0	0	2						
9	MC	BNSK359	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK359	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK359	Yoga	Yoga Teacher									
Total									550	350	900	20	

PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, MC: Mandatory Course (Non-credit), AEC: Ability Enhancement Course, SEC: Skill Enhancement Course, L: Lecture, T: Tutorial, P: Practical S= SDA: Skill Development Activity, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation. K : This letter in the course code indicates common to all the stream of engineering. ESC: Engineering Science Course, ETC: Emerging Technology Course, PLC: Programming Language Course			
.			
Engineering Science Course (ESC/ETC/PLC)			
BUE306A	Sensors and Instrumentation	BUE306C	Operating Systems
BUE306B	Signal Processing	BUE306D	Forensic Science
Ability Enhancement Course – III			
BUEL358A	Applications of 8051 Microcontroller	BUEL358C	PCB Design using EDA Tool
BUE358B	Risk Management in IoT Implementation	BUE358D	Digital Engineering Course (NASSCOM)
Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching– Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23 may please be referred.			
National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.			

VARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.Tech.in Electronics and Computer Engineering**Scheme of Teaching and Examinations 2022**

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2023-24)

IV SEMESTER													
Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	BUE401	Design and Analysis of Algorithms	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
2	IPCC	BUE402	Network Analysis and Control Systems	TD:ECE PSB:ECE	3	0	2		03	50	50	100	4
3	PBL	BUE403	Embedded System Design using ARM	TD:ECE PSB:ECE	2	0	4		03	50	50	100	4
4	PCCL	BUEL404	Algorithms Lab	TD:ECE/CSE PSB:ECE/CSE	0	0	2		03	50	50	100	1
5	ESC	BUE405x	ESC/ETC/PLC	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
6	AEC/ SEC	BUE456x	Ability Enhancement Course/Skill Enhancement Course- IV	TD and PSB: Concerned department	If the course is Theory				01	50	50	100	1
					1	0	0						
					If the course is a lab				02				
					0	0	2						
4	BSC	BBOK407	Biology For Engineers	TD / PSB: BT, CHE,	3	0	0		03	50	50	100	3
7	UHV	BUHK408	Universal human values course	Any Department	1	0	0		01	50	50	100	1
9	MC	BNSK459	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK459	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK459	Yoga	Yoga Teacher									
Total									500	400	900	20	

PCC: Professional Core Course, **PCCL:** Professional Core Course laboratory, **UHV:** Universal Human Value Course, **MC:** Mandatory Course (Non-credit), **AEC:** Ability Enhancement Course, **SEC:** Skill Enhancement Course, **L:** Lecture, **T:** Tutorial, **P:** Practical **S= SDA:** Skill Development Activity, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Evaluation. **K :** This letter in the course code indicates common to all the stream of engineering.

Ability Enhancement Course / Skill Enhancement Course - IV

BUEL456A	Software Tools and Technologies	BUEL456C	Introduction to Raspberry Pi
BUEL456B	Electronic Circuit Application Lab	BUEL456D	Octave /Scilab for Signals

Engineering Science Course (ESC/ETC/PLC)

BUE405A	Linear Integrated Circuits	BUE405C	Data Base Management Systems
BUE405B	Discrete Mathematical Structures and Graph Theory	BUE405D	Web Technologies

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching– Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses is mandatory for the award of degree.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.Tech.in Electronics and Computer Engineering
Scheme of Teaching and Examinations2022
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2023-24)

V SEMESTER													
Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	HSMS	BUE501	Technological Innovation & Entrepreneurship	TD: PSB:	3	0	0		03	50	50	100	3
2	IPCC	BUE502	Object Oriented Programming using JAVA	TD:ECE/CSE PSB:ECE/CSE	3	0	2		03	50	50	100	4
3	PCC	BUE503	Digital System Design using Verilog	TD:ECE PSB:ECE	4	0	0		03	50	50	100	4
4	PCCL	BUE504	Verilog Lab	TD:ECE PSB:ECE	0	0	2		03	50	50	100	1
5	PEC	BUE515x	Professional Elective Course	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
6	PROJ	BUE586	Mini Project	TD:ECE/CSE PSB:ECE/CSE	0	0	4		03	100		100	2
7	AEC	BRMK557	Research Methodology and IPR		2	2	0		02	50	50	100	3
8	MC	BESK508	Environmental Studies		2	0	0		02	50	50	100	2
9	MC	BNSK559	National Service Scheme (NSS)	NSS coordinator	0	0	2			100		100	0
		BPEK559	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK559	Yoga	Yoga Teacher									
Total									500	300	800	22	
Professional Elective Course													
BUE515A		Digital Communication			BUE515C		Software Engineering and Project Management						
BUE515B		Advanced Computer Architecture			BUE515D		Advanced IoT						
PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, MC: Mandatory Course (Non-credit), AEC: Ability													

Enhancement Course, **SEC**: Skill Enhancement Course, **L**: Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **K** : The letter in the course code indicates common to all the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching– Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

Mini-project work: Mini Project is a laboratory-oriented/hands on course that will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications etc. Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of the project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batches mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of the project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

No SEE component for Mini-Project.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering a professional elective is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
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Scheme of Teaching and Examinations 2022
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VI SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	IPCC	BUE601	Computer Networks	TD:ECE/CSE PSB:ECE/CSE	3	0	2		03	50	50	100	4
2	PCC	BUE602	VLSI Design	TD:ECE PSB:ECE	4	0	0		03	50	50	100	4
3	PEC	BUE613x	Professional Elective Course	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
4	OEC	BUE654x	Open Elective Course	TD:ECE PSB:ECE	3	0	0		03	50	50	100	3
5	PROJ	BUE685	Project Phase I	TD:ECE/CSE PSB:ECE/CSE	0	0	4		03	100	--	100	2
6	PCCL	BUEL606	VLSI Laboratory	TD:ECE PSB:ECE	0	0	2		03	50	50	100	1
7	AEC/SDC	BUE657x	Ability Enhancement Course/Skill Development Course V		If the course is offered as a Theory				01	50	50	100	1
					1	0	0						
					If course is offered as a practical								
					0	0	2						
8	MC	BNSK658	National Service Scheme (NSS)	NSS coordinator	0	0	2		100	---	100	0	
		BPEK658	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK658	Yoga	Yoga Teacher									
9	IKS	BIKS609	Indian Knowledge System		1	0	0			100	0	100	00
Total									500	300	800	18	
Professional Elective Course													
BUE613A		Information Theory and Coding				BUE613C		Data Science					
BUE613B		ASIC Design				BUE613D		Cryptography and Network Security					

Open Elective Course			
BUE654A	Fundamentals of Embedded Systems	BUE654C	Microprocessors and Microcontrollers
BUE654B	Introduction to VLSI Circuits and Systems	BUE654D	Electronic Instrumentation
Ability Enhancement Course / Skill Enhancement Course-V			
BUE657A	Latex Software	BUEL657C	Advanced Python Programming
BUE657B	Aptitude – Verbal, Numerical and Logical Reasoning	BUEL657D	Web Programming
PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, MC: Mandatory Course (Non-credit), AEC: Ability Enhancement Course, SEC: Skill Enhancement Course, L: Lecture, T: Tutorial, P: Practical S= SDA: Skill Development Activity, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation. K : The letter in the course code indicates common to all the stream of engineering. PROJ: Project /Mini Project. PEC: Professional Elective Course. PROJ: Project Phase -I, OEC: Open Elective Course Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching– Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23 National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree. Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10. Open Elective Courses: Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum numbers of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10. Project Phase-I : Students have to discuss with the mentor /guide and with their helphe/she has to complete the literature survey and prepare the report and finally			

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VII SEMESTER (Swappable VII and VIII SEMESTER)

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	IPCC	BUE701	Principles of AI and ML	TD:ECE/CSE PSB:ECE/CSE	3	0	2		03	50	50	100	4
2	IPCC	BUE702	System Verilog	TD:ECE PSB:ECE	3	0	2		03	50	50	100	4
3	PCC	BUE703	Computer Graphics and Image Processing	TD:ECE/CSE PSB:ECE/CSE	4	0	0		03	50	50	100	4
4	PEC	BUE714x	Professional Elective Course	TD:ECE/CSE PSB:ECE/CSE	3	0	0		03	50	50	100	3
5	OEC	BUE755x	Open Elective Course	TD:ECE PSB:ECE	3	0	0		03	50	50	100	3
6	PROJ	BUE786	Major Project Phase-II	TD:ECE/CSE PSB:ECE/CSE	0	0	12		03	100	100	200	6
										350	350	700	24

Professional Elective Course

BUE714A	Low Power VLSI Design	BUE714C	Cloud Computing
BUE714B	RISK-V Processor	BUE714D	Big Data Analytics

Open Elective Course

BUE755A	Verilog HDL	BUE755C	ARM Microcontroller
BUE755B	Computer Organization	BUE755D	Operational Amplifiers

PPC: Professional Core Course, **PPCL:** Professional Core Course laboratory, **PEC:** Professional Elective Course, **OEC:** Open Elective Course **PR:** Project Work, **L:** Lecture, **T:** Tutorial, **P:** Practical **S= SDA:** Skill Development Activity, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Evaluation. **TD-** Teaching Department, **PSB:** Paper Setting department, **OEC:** Open Elective Course, **PEC:** Professional Elective Course. **PROJ:** Project work

Note: VII and VIII semesters of IV years of the program

(1) Institutions can swap the VII and VIII Semester Schemes of Teaching and Examinations to accommodate research internships/ industry

internships after the VI semester.

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether the VII or VIII semesters is completed during the beginning of the IV year or the later part of IV years of the program.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum numbers of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

PROJECT WORK (21XXP75): The objective of the Project work is

- (i)** To encourage independent learning and the innovative attitude of the students.
- (ii)** To develop interactive attitude, communication skills, organization, time management, and presentation skills.
- (iii)** To impart flexibility and adaptability.
- (iv)** To inspire team working.
- (v)** To expand intellectual capacity, credibility, judgment and intuition.
- (vi)** To adhere to punctuality, setting and meeting deadlines.
- (vii)** To install responsibilities to oneself and others.
- (viii)** To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of the project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

I Semester

Course Title:	Mathematics-I for Electrical & Electronics Engineering Stream		
Course Code:	BMATE101	CIE Marks	50
Course Type (Theory/Practical/Integrated)	Integrated	SEE Marks	50
		Total Marks	100
Teaching Hours/Week (L:T:P: S)	2:2:2:0	Exam Hours	03
Total Hours of Pedagogy	40 hours Theory + 10 to 12 Lab slots	Credits	04
Course objectives: The goal of the course Mathematics-I for Electrical & Electronics Engineering stream (22MATE11) is to • Familiarize the importance of calculus associated with one variable and multivariable for Electrical and Electronics engineering. • Analyze Electrical and Electronics engineering problems by applying Ordinary Differential Equations. • Familiarize the important tools in Integral Calculus that are essential in Electrical and Electronics engineering. • Develop the knowledge of Linear Algebra to solve the system of equations.			
Teaching-Learning Process Pedagogy (General Instructions): These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied mathematical skills. 2. State the need for Mathematics with Engineering Studies and Provide real-life examples. 3. Support and guide the students for self-study. 4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress. 5. Encourage the students to group learning to improve their creative and analytical skills. 6. Show short related video lectures in the following ways: • As an introduction to new topics (pre-lecture activity). • As a revision of topics (post-lecture activity). • As additional examples (post-lecture activity). • As an additional material of challenging topics (pre-and post-lecture activity). • As a model solution of some exercises (post-lecture activity).			
Module-1: Calculus (8 hours)			
Introduction to polar coordinates and curvature relating to EC & EE Engineering applications. Polar coordinates, Polar curves, angle between the radius vector and the tangent, angle between two curves. Pedal equations. Curvature and Radius of curvature - Cartesian, Parametric, Polar and Pedal forms. Problems. Self-study: Center and circle of curvature, evolutes and involutes. Applications: Communication signals, Manufacturing of microphones, and Image processing. (RBT Levels: L1, L2 and L3)			
Module-2: Series Expansion and Multivariable Calculus (8 hours)			

Introduction of series expansion and partial differentiation in EC & EE Engineering applications.

Taylor's and Maclaurin's series expansion for one variable (Statement only) – problems. Indeterminate forms - L'Hospital's rule - Problems.

Partial differentiation, total derivative - differentiation of composite functions. Jacobian and problems. Maxima and minima for a function of two variables. Problems.

Self-study: Euler's Theorem and problems. Method of Lagrange's undetermined multipliers with single constraint.

Applications: Series expansion in communication signals, Errors and approximations, and vector calculus.

(RBT Levels: L1, L2 and L3)

Module-3: Ordinary Differential Equations (ODEs) of First Order (8 hours)

Introduction to first-order ordinary differential equations pertaining to the applications for EC & EE engineering.

Linear and Bernoulli's differential equations. Exact and reducible to exact differential equations- Integrating factors on $\frac{1}{N} \left(\frac{\partial M}{\partial y} - \frac{\partial N}{\partial x} \right)$ and $\frac{1}{M} \left(\frac{\partial N}{\partial x} - \frac{\partial M}{\partial y} \right)$. Orthogonal trajectories, L-R and C-R circuits. Problems.

Non-linear differential equations: Introduction to general and singular solutions, Solvable for p only, Clairaut's equations, reducible to Clairaut's equations. Problems.

Self-Study: Applications of ODEs, Solvable for x and y.

Applications of ordinary differential equations: Rate of Growth or Decay, Conduction of heat.

(RBT Levels: L1, L2 and L3)

Module-4: Integral Calculus (8 hours)

Introduction to Integral Calculus in EC & EE Engineering applications.

Multiple Integrals: Evaluation of double and triple integrals, evaluation of double integrals by change of order of integration, changing into polar coordinates. Applications to find Area and Volume by double integral. Problems.

Beta and Gamma functions: Definitions, properties, relation between Beta and Gamma functions. Problems.

Self-Study: Volume by triple integration, Center of gravity.

Applications: Antenna and wave propagation, Calculation of optimum power in electrical circuits, field theory.

(RBT Levels: L1, L2 and L3)

Module-5: Linear Algebra (8 hours)

Introduction of linear algebra related to EC & EE engineering applications.

Elementary row transformation of a matrix, Rank of a matrix. Consistency and Solution of system of linear equations - Gauss-elimination method, Gauss-Jordan method and approximate solution by Gauss-Seidel method. Eigenvalues and Eigenvectors, Rayleigh's power method to find the dominant Eigenvalue and Eigenvector.

Self-Study: Solution of system of equations by Gauss-Jacobi iterative method. Inverse of a square matrix by Cayley-Hamilton theorem.

Applications of Linear Algebra: Network Analysis, Markov Analysis, Critical point of a network system. Optimum solution.

(RBT Levels: L1, L2 and L3)

List of Laboratory experiments (2 hours/week per batch/ batch strength 15)

10 lab sessions + 1 repetition class + 1 Lab Assessment

1	2D plots for Cartesian and polar curves
2	Finding angle between polar curves, curvature and radius of curvature of a given curve
3	Finding partial derivatives and Jacobian
4	Applications to Maxima and Minima of two variables
5	Solution of first-order ordinary differential equation and plotting the solution curves
6	Program to compute area, volume and centre of gravity
7	Evaluation of improper integrals
8	Numerical solution of system of linear equations, test for consistency and graphical representation
9	Solution of system of linear equations using Gauss-Seidel iteration
10	Compute eigenvalues and eigenvectors and find the largest and smallest eigenvalue by Rayleigh power method.

Suggested software's: Mathematica/MatLab/Python/Scilab

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

CO1	apply the knowledge of calculus to solve problems related to polar curves and learn the notion of partial differentiation to compute rate of change of multivariate functions
CO2	analyze the solution of linear and nonlinear ordinary differential equations
CO3	apply the concept of change of order of integration and variables to evaluate multiple integrals and their usage in computing area and volume
CO4	make use of matrix theory for solving the system of linear equations and compute eigenvalues and eigenvectors
CO5	familiarize with modern mathematical tools namely MATHEMATICA/ MATLAB/ PYTHON/SCILAB

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation(CIE):

The CIE marks for the theory component of the IC shall be **30 marks** and for the laboratory component **20 Marks**.

CIE for the theory component of the IC

- Three Tests each of 20 Marks; after the completion of the syllabus of 35-40%, 65-70%, and 90-100% respectively.
- Two Assignments/two quizzes/ seminars/one field survey and report presentation/one-course

project totalling 20 marks.

Total Marks scored (test + assignments) out of 80 shall be scaled down to **30 marks**

CIE for the practical component of the IC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15th week of the semester/after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to **05 marks**.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IC/IPCC for **20 marks**.

- The minimum marks to be secured in CIE to appear for SEE shall be 12 (40% of maximum marks) in the theory component and 08 (40% of maximum marks) in the practical component. The laboratory component of the IC/IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 05 questions is to be set from the practical component of IC/IPCC, the total marks of all questions should not be more than 25 marks.

The theory component of the IC shall be for both CIE and SEE.

Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English/Kannada). The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks. The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks**.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Books (Title of the Book/Name of the author/Name of the publisher/Edition and Year)

Text Books

1. **B. S. Grewal:** "Higher Engineering Mathematics", Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig:** "Advanced Engineering Mathematics", John Wiley & Sons, 10thEd., 2018.

Reference Books

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed., 2017
2. **Srimanta Pal & Subodh C.Bhunia:** "Engineering Mathematics" Oxford University Press,

3rd Ed., 2016.

3. **N.P Bali and Manish Goyal:** “A Textbook of Engineering Mathematics” Laxmi Publications, 10th Ed., 2022.
4. **C. Ray Wylie, Louis C. Barrett:** “Advanced Engineering Mathematics” McGraw – Hill Book Co., New York, 6th Ed., 2017.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** “Engineering Mathematic for Semester I and II”, Mc-Graw Hill Education(India) Pvt. Ltd 2015.
6. **H. K. Dass and Er. Rajnish Verma:** “Higher Engineering Mathematics” S. Chand Publication, 3rd Ed., 2014.
7. **James Stewart:** “Calculus” Cengage Publications, 7thEd., 2019.
8. **David C Lay:** “Linear Algebra and its Applications”, Pearson Publishers, 4th Ed., 2018.
9. **Gareth Williams:** “Linear Algebra with Applications”, Jones Bartlett Publishers Inc., 6th Ed., 2017.
10. **Gilbert Strang:** “Linear Algebra and its Applications”, Cengage Publications, 4th Ed. 2022.

Web links and Video Lectures (e-Resources):

- <http://nptel.ac.in/courses.php?disciplineID=111>
- [http://www.class-central.com/subject/math\(MOOCs\)](http://www.class-central.com/subject/math(MOOCs))
- <http://academicearth.org/>
- VTU e-Shikshana Program
- VTU EDUSAT Program

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminar

COs and POs Mapping (Individual teacher has to fill up)

COs	POs						
	1	2	3	4	5	6	7
CO1							
CO2							
CO3							
CO4							
CO5							

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

II Semester

Course Title:	Mathematics-II for Electrical & Electronics Engineering Stream		
Course Code:	BMATE201	CIE Marks	50
Course Type (Theory/Practical/Integrated)	Integrated	SEE Marks	50
		Total Marks	100
Teaching Hours/Week (L:T:P: S)	2:2:2:0	Exam Hours	03
Total Hours of Pedagogy	40 hours Theory + 10 to 12 Lab slots	Credits	04
Course objectives: The goal of the course Mathematics-II for Electrical & Electronics Engineering Stream (22MATE21) is to • Familiarize the importance of Vector calculus, Vector Space and Linear transformation for electronics and electrical engineering. • Have an insight into solving ordinary differential equations by using Laplace transform techniques. • Develop the knowledge of solving electronics and electrical engineering problems numerically.			
Teaching-Learning Process Pedagogy (General Instructions): These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied mathematical skills. 2. State the need for Mathematics with Engineering Studies and Provide real-life examples. 3. Support and guide the students for self-study. 4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress. 5. Encourage the students to group learning to improve their creative and analytical skills. 6. Show short related video lectures in the following ways: • As an introduction to new topics (pre-lecture activity). • As a revision of topics (post-lecture activity). • As additional examples (post-lecture activity). • As an additional material of challenging topics (pre-and post-lecture activity). • As a model solution of some exercises (post-lecture activity).			
Module-1: Vector Calculus (8 hours)			

Introduction to Vector Calculus in EC & EE engineering applications.

Vector Differentiation: Scalar and vector fields. Gradient, directional derivative, curl and divergence - physical interpretation, solenoidal and irrotational vector fields. Problems.

Vector Integration: Line integrals, Surface integrals. Applications to work done by a force and flux. Statement of Green's theorem and Stoke's theorem. Problems.

Self-Study: Volume integral and Gauss divergence theorem.

Applications: Conservation of laws, Electrostatics, Analysis of streamlines and electric potentials.

(RBT Levels: L1, L2 and L3)

Module-2: Vector Space and Linear Transformations(8 hours)**Importance of Vector Space and Linear Transformations in the field of EC & EE engineering applications.**

Vector spaces: Definition and examples, subspace, linear span, Linearly independent and dependent sets, Basis and dimension.

Linear transformations: Definition and examples, Algebra of transformations, Matrix of a linear transformation. Change of coordinates, Rank and nullity of a linear operator, Rank-Nullity theorem. Inner product spaces and orthogonality.

Self-study: Angles and Projections. Rotation, reflection, contraction and expansion.

Applications: Image processing, AI & ML, Graphs and networks, Computer graphics.

(RBT Levels: L1, L2 and L3)

Module-3: Laplace Transform(8 hours)**Importance of Laplace Transform for EC & EE engineering applications.**

Existence and Uniqueness of Laplace transform (LT), transform of elementary functions, region of convergence. Properties—Linearity, Scaling, t-shift property, s-domain shift, differentiation in the s-domain, division by t, differentiation and integration in the time domain. LT of special functions—periodic functions (square wave, saw-tooth wave, triangular wave, full & half wave rectifier), Heaviside Unit step function, Unit impulse function.

Inverse Laplace Transforms:

Definition, properties, evaluation using different methods, convolution theorem (without proof), problems, and applications to solve ordinary differential equations.

Self-Study: Verification of convolution theorem.

Applications: Signals and systems, Control systems, LR, CR & LCR circuits.

(RBT Levels: L1, L2 and L3)

Module-4: Numerical Methods -1(8 hours)**Importance of numerical methods for discrete data in the field of EC & EE engineering applications.**

Solution of algebraic and transcendental equations: Regula-Falsi method and Newton-Raphson method (only formulae). Problems.

Finite differences, Interpolation using Newton's forward and backward difference formulae, Newton's divided difference formula and Lagrange's interpolation formula (All formulae without proof). Problems.

Numerical integration: Trapezoidal, Simpson's $(1/3)^{\text{rd}}$ and $(3/8)^{\text{th}}$ rules (without proof). Problems.

Self-Study: Bisection method, Lagrange's inverse Interpolation, Weddle's rule.

Applications: Estimating the approximate roots, extremum values, area, volume, and surface area.
(RBT Levels: L1, L2 and L3)

Module-5:Numerical Methods -2(8 hours)

Introduction to various numerical techniques for handling EC & EE applications.

Numerical Solution of Ordinary Differential Equations (ODEs):

Numerical solution of ordinary differential equations of first order and first degree - Taylor's series method, Modified Euler's method, Runge-Kutta method of fourth order and Milne's predictor-corrector formula (No derivations of formulae). Problems.

Self-Study: Adam-Bashforth method.

Applications: Estimating the approximate solutions of ODE for electric circuits.

(RBT Levels: L1, L2 and L3)

List of Laboratory experiments (2 hours/week per batch/ batch strength 15)

10 lab sessions + 1 repetition class + 1 Lab Assessment

1	Finding gradient, divergent, curl and their geometrical interpretation and Verification of Green's theorem
2	Computation of basis and dimension for a vector space and Graphical representation of linear transformation
3	Visualization in time and frequency domain of standard functions
4	Computing inverse Laplace transform of standard functions
5	Laplace transform of convolution of two functions
6	Solution of algebraic and transcendental equations by Regula-Falsi and Newton-Raphson method
7	Interpolation/Extrapolation using Newton's forward and backward difference formula
8	Computation of area under the curve using Trapezoidal, Simpson's $(1/3)^{rd}$ and $(3/8)^{th}$ rule
9	Solution of ODE of first order and first degree by Taylor's series and Modified Euler's method
10	Solution of ODE of first order and first degree by Runge-Kutta 4 th order and Milne's predictor-corrector method

Suggested software's: Mathematica/MatLab/Python/Scilab

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

CO1	Understand the applications of vector calculus refer to solenoidal, irrotational vectors, lineintegral and surface integral.
CO2	Demonstrate the idea of Linear dependence and independence of sets in the vector space, and linear transformation
CO3	To understand the concept of Laplace transform and to solve initial value problems.
CO4	Apply the knowledge of numerical methods in solving physical and engineering phenomena.
CO5	Get familiarize with modern mathematical tools namely MATHEMATICA/MATLAB/PYTHON/ SCILAB

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation(CIE):

The CIE marks for the theory component of the IC shall be **30 marks** and for the laboratory component **20 Marks**.

CIE for the theory component of the IC

- Three Tests each of 20 Marks; after the completion of the syllabus of 35-40%, 65-70%, and 90-100% respectively.
- Two Assignments/two quizzes/ seminars/one field survey and report presentation/one-course project totalling 20 marks.

Total Marks scored (test + assignments) out of 80 shall be scaled down to **30 marks**

CIE for the practical component of the IC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to **05 marks**.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IC/IPCC for **20 marks**.

- The minimum marks to be secured in CIE to appear for SEE shall be 12 (40% of maximum marks) in the theory component and 08 (40% of maximum marks) in the practical component. The laboratory component of the IC/IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 05 questions is

to be set from the practical component of IC/IPCC, the total marks of all questions should not be more than 25 marks.

The theory component of the IC shall be for both CIE and SEE.

Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English/Kannada). The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks. The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks.**
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Books (Title of the Book/Name of the author/Name of the publisher/Edition and Year)

Text Books

1. **B. S. Grewal:** “Higher Engineering Mathematics”, Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig:** “Advanced Engineering Mathematics”, John Wiley & Sons, 10thEd., 2018.

Reference Books

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4. **C. Ray Wylie, Louis C. Barrett:** “Advanced Engineering Mathematics” McGraw – Hill Book Co., New York, 6th Ed., 2017.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** “Engineering Mathematic for Semester I and II”, Mc-Graw Hill Education(India) Pvt. Ltd 2015.
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7. **James Stewart:** “Calculus” Cengage Publications, 7thEd., 2019.
8. **David C Lay:** “Linear Algebra and its Applications”, Pearson Publishers, 4th Ed., 2018.
9. **Gareth Williams:** “Linear Algebra with applications”, Jones Bartlett Publishers Inc., 6th Ed., 2017.
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Web links and Video Lectures (e-Resources):

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- [http://www.class-central.com/subject/math\(MOOCs\)](http://www.class-central.com/subject/math(MOOCs))
- <http://academicearth.org/>
- VTU e-Shikshana Program
- VTU EDUSAT Program

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Quizzes
- Assignments
- Seminar

COs and POs Mapping (Individual teacher has to fill up)

COs	POs						
	1	2	3	4	5	6	7
CO1							
CO2							
CO3							
CO4							
CO5							

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

Course Title:	Applied Physics for EEE Stream		
Course Code:	BPHE102/202	CIE Marks	50
Course Type (Theory/Practical/Integrated)	Integrated	SEE Marks	50
		Total Marks	100
Teaching Hours/Week (L:T:P: S)	2:2:2:0	Exam Hours	03
Total Hours of Pedagogy	40 hours+10-12 Lab Slots	Credits	04
Course objectives - To study the principles of quantum mechanics - To understand the properties of dielectrics and superconductors - To study the essentials of photonics for engineering applications. - To understand fundamentals of vector calculus and EM waves. - To study the knowledge about semiconductors and devices.			
Teaching-Learning Process These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes and make Teaching –Learning more effective 1. Flipped Class 2. Chalk and Talk 3. Blended Mode of Learning 4. Simulations, Interactive Simulations and Animations 5. NPTEL and Other Videos for theory topics 6. Smart Class Room 7. Lab Experiment Videos			
Module-1 (08 Hours)			
Quantum Mechanics: de Broglie Hypothesis and Matter Waves, de Broglie wavelength and derivation of expression by analogy, Phase Velocity and Group Velocity, Heisenberg's Uncertainty Principle and its application (Non existence of electron inside the nucleus-Non Relativistic), Principle of Complementarity, Wave Function, Time independent Schrödinger wave equation, Physical Significance of a wave function and Born Interpretation, Expectation value, Eigen functions and Eigen Values, Particle inside one dimensional infinite potential well, Waveforms and Probabilities. Numerical Problems Pre-requisite: Wave–Particle dualism Self-learning: de Broglie Hypothesis			
Module-2 (08 hours)			
Electrical Properties of Solids: Conductors: Quantum Free Electron Theory of Metals: Assumptions, Fermi-energy, Fermi factor, Variation of Fermi Factor with Temperature and Energy, Mention of expression for electrical conductivity. Dielectric Properties: Polar and non-polar dielectrics, Electrical Polarization Mechanisms, internal fields in solids, Clausius-Mossotti equation (Derivation), Solid, Liquid and Gaseous dielectrics. Application of dielectrics in transformers, Capacitors, Electrical Insulation. Numerical Problems. Superconductivity: Introduction to Superconductors, Temperature dependence of resistivity, Meissner Effect, Critical Field, Temperature dependence of Critical field, Types of Super Conductors, BCS theory (Qualitative), High Temperature superconductivity, SQUID, MAGLEV, Numerical problems. Pre-requisites: Classical Free Electron Theory Self-learning: Dielectrics Basics			
Module-3 (08 hours)			
Lasers and Optical Fibers: Lasers: Characteristics of LASER, Interaction of radiation with matter, Expression for Energy Density and its significance. Requisites of a Laser System. Conditions for Laser action. Principle, Construction and Working of Carbon Dioxide Laser. Application of Lasers in Defense (Laser range finder) and Laser Printing. Numerical			

Problems	
Optical Fibers: Total Internal Reflection, Propagation mechanism, Angle of Acceptance, Numerical Aperture, Fractional Index Change, Modes of Propagation, Number of Modes and V Number, Types of Optical Fibers. Attenuation and Mention of Expression for Attenuation coefficient, Attenuation Spectrum of an Optical Fiber with Optical Windows. Discussion of Block Diagram of Point to Point Communication, Intensity based Fiber Optic Displacement Sensor, Merits and Demerits, Numerical problems. Pre-requisite: Properties of light Self-learning: Total Internal Reflection	
Module-4 (08 hours)	
Maxwell's Equations and EM waves: Maxwell's Equations: Fundamentals of Vector Calculus. Divergence and Curl of Electric field and Magnetic field (static), Gauss' divergence theorem and Stoke's theorem. Description of laws of Electrostatics, Magnetism, Faraday's laws of EMI, Current Density, Equation of Continuity, Displacement Current (with derivation), Maxwell's equations in vacuum, Numerical Problems EM Waves: The wave equation in differential form in free space (Derivation of the equation using Maxwell's equations), Plane Electromagnetic Waves in vacuum, their transverse nature. Pre-requisite: Electricity & Magnetism Self-learning: Fundamentals of vector calculus.	
Module-5 (08 hours)	
Semiconductors and Devices: Fermi level in Intrinsic & Extrinsic Semiconductor, Expression for concentration of electrons in conduction band & holes concentration in valance band (only mention the expression), Relation between Fermi energy & Energy gap in intrinsic semiconductors (derivation), Law of mass action, Electrical conductivity of a semiconductor (derivation), Hall effect, Expression for Hall coefficient (derivation) and its application. Photo-diode and Power responsivity, Construction and working of Semiconducting Laser, Four probe method to determine resistivity, Phototransistor, Numerical problems. Pre-requisite: Basics of Semiconductors Self-learning: Fermi level in Intrinsic & Extrinsic Semiconductor	
Course outcome (Course Skill Set) At the end of the course the student will be able to:	
CO1	Describe the fundamental principles of the Quantum Mechanics and the essentials of Photonics.
CO2	Elucidate the concepts of conductors, dielectrics and superconductivity
CO3	Discuss the fundamentals of vector calculus and their applications in Maxwell's Equations and EM Waves.
CO4	Summarize the properties of semiconductors and the working principles of semiconductor devices.
CO5	Practice working in groups to conduct experiments in physics and Perform precise and honest measurements.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation (CIE): The CIE marks for the theory component of the IC shall be 30 marks and for the laboratory component 20 Marks. CIE for the theory component of the IC - Three Tests each of 20 Marks; after the completion of the syllabus of 35-40%, 65-70%, and 90-100% respectively. - Two Assignments/two quizzes/ seminars/one field survey and report presentation/one-course project totalling 20 marks.	

Total Marks scored (test + assignments) out of 80 shall be scaled down to **30 marks**

CIE for the practical component of the IC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to **05 marks**.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IC/IPCC for **20 marks**.

- The minimum marks to be secured in CIE to appear for SEE shall be 12 (40% of maximum marks) in the theory component and 08 (40% of maximum marks) in the practical component. The laboratory component of the IC/IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 05 questions is to be set from the practical component of IC/IPCC, the total marks of all questions should not be more than 25 marks.

The theory component of the IC shall be for both CIE and SEE.

Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English/Kannada. The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks. The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks**.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Books (Title of the Book/Name of the author/Name of the publisher/Edition and Year)

1. A Textbook of Engineering Physics- M.N. Avadhanulu and P.G. Kshirsagar, 10th revised Ed, S. Chand. & Company Ltd, New Delhi.
2. An Introduction to Lasers theory and applications by M.N.Avadhanulu and P.S. Hemne revised Edition 2012. S. Chand and Company Ltd -New Delhi.
3. Engineering Physics-Gaur and Gupta-Dhanpat Rai Publications-2017.
4. Concepts of Modern Physics-Arthur Beiser: 6th Ed;Tata McGraw Hill Edu Pvt Ltd- New Delhi 2006.
5. Fundamentals of Fibre Optics in Telecommunication & Sensor Systems, B.P. Pal, New Age International Publishers.
6. Introduction to Electrodynamics, David Griffith, 4th Edition, Cambridge University Press 2017.
7. Lasers and Non Linear Optics – B.B. Laud, 3rd Ed, New Age International Publishers 2011.
8. LASERS Principles, Types and Applications by K.R. Nambiar-New Age International Publishers.
9. Solid State Physics-S O Pillai, 8th Ed- New Age International Publishers-2018.

Web links and Video Lectures (e-Resources):

Laser:https://www.britannica.com/technology/laser_k

Laser:<https://nptel.ac.in/courses/115/102/115102124/>

Quantum mechanics:<https://nptel.ac.in/courses/115/104/115104096/>

Physics:<http://hyperphysics.phy-astr.gsu.edu/hbase/hframe.html>

Numerical Aperture of fiber:<https://bop-iitk.vlabs.ac.in/exp/numerical-aperture-measurement>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

<http://nptel.ac.in>

<https://swayam.gov.in>

<https://www.vlab.co.in/participating-institute-amrita-vishwa-vidyapeetham>

<https://vlab.amrita.edu/index.php?sub=1&brch=189&sim=343&cnt=1>

https://virtuallabs.merlot.org/vl_physics.html

<https://phet.colorado.edu>

<https://www.mypysicslab.com>

Laboratory Component:

Any Ten Experiments have to be completed from the list of experiments

Note: The experiments have to be classified into

- a) Exercise
- b) Demonstration
- c) Structured Inquiry
- d) Open Ended

Based on the convenience classify the following experiments into above categories selecting at least three experiments for each type. Select at least one simulation/spreadsheet activity.

List of Experiments

1. Determination of wavelength of LASER using Diffraction Grating.
2. Determination of acceptance angle and numerical aperture of the given Optical Fiber.
3. Determination of Magnetic Flux Density at any point along the axis of a circular coil.
4. Determination of resistivity of a semiconductor by Four Probe Method
5. Study the I-V Characteristics of the Given Bipolar Junction Transistor.
6. Determination of dielectric constant of the material of capacitor by Charging and Discharging method.
7. Study the Characteristics of a Photo-Diode and to determine the power responsivity / Verification of Inverse Square Law of Intensity of Light.
8. Study the frequency response of Series & Parallel LCR circuits.
9. Determination of Plank's Constant using LEDs.
10. Determination of Fermi Energy of Copper.
11. Identification of circuit elements in a Black Box and determination of values of the components.
12. Determination of Energy gap of the given Semiconductor.
13. Step Interactive Physical Simulations.
14. Study of motion using spread Sheets
15. Study of Application of Statistics using spread sheets
16. PHET Interactive

Simulations(<https://phet.colorado.edu/en/simulations/filter?subjects=physics&type=html,prototype>)

COs and POs Mapping (Individual teacher has to fill up)

COs	POs											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1	3	2	-	-	-	-	-	-	-	-	-	2
CO2	3	2	-	-	-	-	-	-	-	-	-	2
CO3	3	2	-	-	-	-	-	-	-	-	-	2
CO4	3	2	-	-	1	-	-	-	-	-	-	2
CO5	3	2	1	-	2	-	-	3	3	-	-	2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped

Note : The CO-PO mapping values are indicative. The course coordinator can alter the mapping using **Competency and Performance Indicators** mentioned in the **AICTE Exam reforms**.

Electrical & Electronics Engineering and Allied branches(Chemistry group)

CourseTitle:	Chemistry for Electrical and Electronics Engineering stream		
CourseCode:	BCHEE202/202	CIEMarks	50
Course Type(Theory/Practical/Integrated)	Integrated	SEEMarks	50
		Total Marks	100
TeachingHours/Week(L:T:P:S) ¹	2:2:2:0	Exam Hours	03
TotalHoursofPedagogy	40hoursTheory+10to 12Lab slots	Credits	04
Courseobjectives - Toenablestudentstoacquireknowledgeonprinciplesofchemistryforengineeringapplications. - Todevelopanintuitiveunderstandingofchemistrybyemphasizingtherelatedbranchesofengineering. - Toprovidestudentswithasolidfoundationinanalyticalreasoningrequiredtosolvesocietal problems.			
Teaching-LearningProcess Thesearesamplestrategies,whichteachercanusetoacceleratetheattainmentofthevariouscourseoutcomesandmakeTeaching-Learningmoreeffective - Tutorial&remedialclassesforneedystudents(notregularT/R) - ConductingMakeupclasses/Bridgecoursesforneedystudents - Demonstrationofconceptseitherbybuildingmodelsorbyindustryvisit - Experimentsinlaboratoriesshallbeexecutedinblendedmode(conventionalornon-conventionalmethods) - UseofICT-Onlinevideos,onlinecourses - Useofonlineplatformsforassignments/Notes/Quizzes(Ex.Googleclassroom)			
MODULE1:ChemistryofElectronicMaterials(8hr)			
ConductorsandInsulators: Introduction,principlewithexamples. Semiconductors: Introduction, production of electronic grade silicon-Czochralski process(CZ) andFloatZone(FZ)methods. Polymers: Introduction,Molecularweight-Numberaverage,Weightaverageandnumericalproblems.Conductingpolymers-synthesisandconductingmechanismofpolyacetylene.Preparation, propertiesandcommercialapplicationsofgrapheneoxide. PCB: Electroless plating – Introduction, Electroless plating of copper in the manufacture ofdouble-sidedPCB. Self-learning: Technologicalimportanceofmetalfinishinganddistinctionbetween electroplatingandelectrolessplating.			
MODULE2:EnergyConversionandStorage(8hr)			
Batteries: Introduction, classification of batteries. Components, construction, working andapplications of modern batteries; Na-ion battery, solid state battery (Li-polymer battery)andflowbattery(Vanadiumredoxflowbattery). FuelCells: Introduction,construction,workingandapplicationsofmethanol-oxygenand			

1.NOTE:Whereverthecontact hoursisnotsufficient,tutorialhourcanbeconvertedto theoryhours

polymerelectrolytemembrane(PEM)fuelcell.

SolarEnergy:Introduction,importanceofsolarPVcell,constructionandworkingofsolarPVcell,advantagesanddisadvantages.

Self-learning:Electrodesforelectrostaticdoublelayercapacitors,pseudocapacitors,and hybridcapacitor.

MODULE3:CorrosionScienceandE-wasteManagement(8hr)

CorrosionChemistry:Introduction,electrochemicaltheoryofcorrosion,typesofcorrosion-differentialmetalanddifferentialaeration.Corrosioncontrol-galvanization,anodization and sacrificial anode method. Corrosion Penetration Rate (CPR) - Introductionandnumerical problem.

E-waste Management: Introduction, sources, types, effects of e-waste on environment andhuman health, methods of disposal, advantages of recycling. Extraction of copper and goldfrome-waste.

Self-learning:RecyclingofPCBandbatterycomponents

MODULE4:NanomaterialsandDisplaySystems(8hr)

Nanomaterials: Introduction, size dependent properties of nanomaterials (Surface area,Catalytic, Conducting), preparation of nanomaterials by sol-gel and co-precipitation methodwithexample.Introduction,propertiesandapplications- Nanofibers,Nanophotonics,Nanosensors.

DisplaySystems:Liquidcrystals(LC's)-Introduction,classification,propertiesandapplication in Liquid Crystal Displays (LCD's). Properties and application of Organic LightEmittingDiodes(OLED's)andQuantumLightemittingdiodes(QLED's).

PerovskiteMaterials:Introduction,propertiesandapplicationsinoptoelectronicdevices.

Self-learning:Properties&electrochemicalapplicationsofcarbonnanotubesandgraphene.

MODULE5:SensorsinAnalyticalTechniques(8hr)

Electrode System: Introduction, types of electrodes. Ion selective electrode – definition,construction, working and applications of glass electrode. Determination of pH using glasselectrode. Reference electrode- Introduction, calomel electrode– construction, workingand applicationsof calomelectrode.Concentrationcell– Definition,constructionandNumericalproblems.

Sensors:Introduction,workingprincipleandapplicationsofConductometricsensors,Electrochemicalsensors, Thermometricsensors, andOpticalsensors.

AnalyticalTechniques:Introduction,principleandinstrumentationofColorimetricsensors; its application in the estimation of copper, principleandinstrumentationof Potentiometric sensors; principleandinstrumentationof its applicationin the estimation of iron, Conductometric sensors; its application in the estimation of weakacid.

Self-learning:IRandUV-Visiblespectroscopy.

PRACTICALMODULE

A-Demonstration(anytwo)offline/virtual:

A1.Synthesisofpolyurethane

A2. Determination of strength of an acid in Pb-acid

batteryA3.Synthesisofironoxidenanoparticles

A4.Electroplatingofcopperonmetallicobjects

B-Exercise(compulsorilyany4tobeconducted):

- B1. Conductometric estimation of acid mixture
 B2. Potentiometric estimation of FAS using $K_2Cr_2O_7$
 B3. Determination of pK_a of vinegar using pH sensor (Glass electrode)
 B4. Determination of rate of corrosion of mild steel by weight loss method
 B5. Estimation of total hardness of water by EDTA method

C-Structured Enquiry (compulsorilyany4tobeconducted):

- C1. Estimation of Copper present in electroplating effluent by optical sensor (colorimetry)
 C2. Determination of Viscosity coefficient of lubricant (Ostwald's viscometer)
 C3. Estimation of iron in TMT bar by diphenyl amine/external indicator method
 C4. Estimation of Sodium present in soil/effluent sample using flame photometry
 C5. Determination of Chemical Oxygen Demand (COD) of industrial wastewater sample

D-Open Ended Experiments (any two):

- D1. Estimation of metal in e-waste by optical sensors
 D2. Electroless plating of Nickel on Copper
 D3. Determination of glucose by electrochemical sensors
 D4. Synthesis of polyaniline and its conductivity measurement

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

CO1.	Identify the terms and processes involved in scientific and engineering applications
CO2.	Explain the phenomena of chemistry to describe the methods of engineering processes
CO3.	Solve the problems in chemistry that are pertinent in engineering applications
CO4.	Apply the basic concepts of chemistry to explain the chemical properties and processes
CO5.	Analyze properties and multi processes associated with chemical substances in disciplinary situations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

The CIE marks for the theory component of the IC shall be **30 marks** and for the laboratory component **20 Marks**.

CIE for the theory component of the IC

- Three Tests each of 20 Marks; after the completion of the syllabus of 35-40%, 65-70%, and 90-100% respectively.
- Two Assignments/two quizzes/ seminars/one field survey and report presentation/one-course project totalling 20 marks.

Total Marks scored (test + assignments) out of 80 shall be scaled down to **30 marks**

CIE for the practical component of the IC

- On completion of every experiment/program in the laboratory, the students shall be

evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.

- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to **05 marks**.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IC/IPCC for **20 marks**.

- The minimum marks to be secured in CIE to appear for SEE shall be 12 (40% of maximum marks) in the theory component and 08 (40% of maximum marks) in the practical component. The laboratory component of the IC/IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 05 questions is to be set from the practical component of IC/IPCC, the total marks of all questions should not be more than 25 marks.

The theory component of the IC shall be for both CIE and SEE.

Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English/Kannada). The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks. The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks**.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Books(TitleoftheBook/Nameoftheauthor/Nameofthepublisher/EditionandYear)

1. WileyEngineeringChemistry,WileyIndiaPvt.Ltd.NewDelhi,2013-2ndEdition.
2. EngineeringChemistry,Satyaprakash&ManishaAgrawal,KhannaBookPublishing,Delhi
3. ATextBookofEngg.Chemistry,ShashiChawla,DhanpatRai&Co.(P)Ltd.
4. EssentialsofPhysicalChemistry,Bahl & Tuli,S.ChandPublishing
5. AppliedChemistry,SunitaRattan,Kataria5.EngineeringChemistry,Baskar,Wiley
6. EngineeringChemistry-I,D.Grouar Krishana,VikasPublishing
7. ATextbookofEngineeringChemistry,SSDara&Dr.SSUmare,SChand&CompanyLtd.,12thEdition,2011
8. ATextBookofEngineeringChemistry,R.V.GadagandNityanandaShetty,I.K.InternationalPublishinghouse. 2ndEdition,2016.
9. TextBookofPolymerScience,F.W.Billmeyer,JohnWiley&Sons,4thEdition,1999.
10. NanotechnologyAChemicalApproachtoNanomaterials,G.A.Ozin &A.C.Arsenault,RSCPublishing,2005.
11. CorrosionEngineering,M.G.Fontana,N.D.Greene,McGrawHillPublications,NewYork,3rdEdition,1996.
12. Linden'sHandbookofBatteries,KirbyW.Beard,FifthEdition,McGrawHill,2019.
13. OLEDDisplayFundamentalsandApplications,TakatoshiTsujiMura,Wiley-Blackwell,2012
14. Supercapacitors: Materials, Systems, and Applications, Max Lu, Francois Beguin,ElzbietaFrackowiak,Wiley-VCH;1st edition,2013.

15. "Handbook on Electroplating with Manufacture of Electrochemicals", ASIAPACIFIC BUSINESS PRESS Inc., 2017. Dr.H. Panda,
16. Expanding the Vision of Sensor Materials. National Research Council 1995, Washington, DC: The National Academies Press. doi:10.17226/4782.
17. Engineering Chemistry, Edited by Dr. Mahesh Band and Dr. Roopashree B, Sunstar Publisher, Bengaluru, ISBN 978-93-85155-70-3, 2022
18. High Performance Metallic Materials for Cost Sensitive Applications, F.H. Froes, et al. John Wiley & Sons, 2010
19. Instrumental Methods of Analysis, Dr. K. R. Mahadik and Dr. L. Sathiyarayanan, Nirali Prakashan, 2020
20. Principles of Instrumental Analysis, Douglas A. Skoog, F. James Holler, Stanley R. Crouch Seventh Edition, Cengage Learning, 2020
21. Polymer Science, VR Gowariker, NV Viswanathan, Jayadev, Sreedhar, New Age Int. Publishers, 4th Edition, 2021
22. Engineering Chemistry, PC Jain & Monica Jain, Dhanpat Rai Publication, 2015-16th Edition.
23. Nanostructured materials and nanotechnology, Hari Singh, Nalwa, academic press, 1st Edition, 2002.
24. Nanotechnology Principles and Practices, Sulabha Kulkarni, Capital Publishing Company, 3rd Edition 2014
25. Principles of nanotechnology, Phanikumar, Scitech publications, 2nd Edition, 2010.
26. Chemistry for Engineering Students, B.S. Jai Prakash, R. Venugopal, Sivakumaraiah & Pushpalyengar., Subash Publications, 5th Edition, 2014
27. "Engineering Chemistry", O.G. Palanna, Tata McGraw Hill Education Pvt. Ltd. New Delhi, Fourth Reprint, 2015.
28. Chemistry of Engineering materials, Malini S, KS Anantha Raju, CBS publishers Pvt Ltd.
29. Laboratory Manual Engg. Chemistry, Anupma Rajput, Dhanpat Rai & Co.

Web links and Video Lectures (e-Resources):

- <http://libgen.rs/>
- <https://nptel.ac.in/downloads/122101001/>
- <https://nptel.ac.in/courses/104/103/104103019/>
- <https://ndl.iitkgp.ac.in/>
- <https://www.youtube.com/watch?v=faESCxAWR9k>
- <https://www.youtube.com/watch?v=TBqXMWaxZYM&list=PLyhmwFtznRhuz8L1bb3X-9IbHrDMjHWWH>
- <https://www.youtube.com/watch?v=j5Hml6KN4TI>
- <https://www.youtube.com/watch?v=X9GHBdyYcyo>
- <https://www.youtube.com/watch?v=1xWBPZnEjk8>
- <https://www.youtube.com/watch?v=wRAo-M8xBHM>

Activity Based Learning (Suggested Activities in Class) / Practical Based learning

- <https://www.vlab.co.in/broad-area-chemical-sciences>
- <https://demonstrations.wolfram.com/topics.php>
- <https://interestingengineering.com/science>

COs and POs Mapping (Individual teacher has to fill up)

PO												
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	1	1				1					
CO2	3	1	1				1					
CO3	3	1	1				1					
CO4	3	1	1				1					
CO5	3	1	1				1					

16-2-2023

Course Title:	Elements of Electrical Engineering		
Course Code:	BEEE103	CIE Marks	50
Course Type (Theory/Practical /Integrated)	Theory	SEE Marks	50
		Total Marks	100
Teaching Hours/Week (L:T:P: S)	2:2:0:0	Exam Hours	03
Total Hours of Pedagogy	40 hours	Credits	03
Course objectives - To explain the basic laws used in the analysis of DC circuits, electromagnetism. - To explain the behavior of circuit elements in single-phase circuits. - To explain three phase circuits, balanced loads and measurement of three phase power. - To explain the measuring techniques, measuring instruments and domestic wiring. - To explain electricity billing, equipment and personal safety measures.			
Teaching-Learning Process These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes and make Teaching –Learning more effective - Chalk and talk - Animated/NPTEL videos - Cut sections - PPTs			
Module-1 (08 Hrs)			
DC circuits: Ohm's law and Kirchhoff's laws, analysis of series, parallel and series-parallel circuits. Power and energy. Electromagnetism: Faraday's Laws of Electromagnetic Induction, Lenz's Law, Flemings rules, statically and dynamically induced EMF; concepts of self and mutual inductance. Coefficient of Coupling. Energy stored in magnetic field. Simple Numerical.			
Module-2 (08 Hrs)			
Single-phase AC circuits: Generation of sinusoidal voltage, frequency of generated voltage, average value, RMS value, form factor and peak factor of sinusoidal voltage and currents. Phasor representation of alternating quantities. Analysis of R, L, C, R-L, R-C and R-L-C circuits with phasor diagrams, Real power, reactive power, apparent power, and Power factor. Series, Parallel and Series-Parallel circuits. Simple Numerical.			
Module-3 (08 Hrs)			
Three-phase AC circuits: Necessity and advantage of 3-phase system. Generation of 3-phase power. Definition of phase sequence. Balanced supply and balanced load. Relationship between line and phase values of balanced star and delta connections. Power in balanced 3-phase circuits. Measurement of 3-phase power by 2-wattmeter method. Simple Numerical.			
Module-4 (08 Hrs)			
Measuring instruments: construction and working principle of whetstone's bridge, Kelvin's double bridge, Megger, Maxwell's bridge for inductance, Schering's bridge for capacitance, concepts of current transformer and potential transformer. (Only balance equations and Excluding Vector diagram approach) Domestic Wiring: Requirements, Types of wiring: casing, capping. Two way and three way control of load.			
Module-5 (08 Hrs)			
Electricity bill: Power rating of household appliances including air conditioners, PCs, laptops, printers, etc. Definition of "unit" used for consumption of electrical energy, two-part electricity tariff, calculation of electricity bill for domestic consumers. Equipment Safety measures: Working principle of Fuse and Miniature circuit breaker (MCB), merits and demerits. Personal safety measures: Electric Shock, Earthing and its types, Safety Precautions to avoid shock, and Residual Current Circuit Breaker (RCCB) and Earth Leakage Circuit Breaker (ELCB).			

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

C01	Understand the concepts of DC circuits and Electromagnetism.
C02	Understand the concepts of single phase and Three phase AC circuits.
C03	Apply the basic Electrical laws to solve circuits.
C04	Understand the concepts of measurements and measuring Instruments
C05	Explain the concepts of domestic wiring, electricity billing, circuit protective devices and personal safety measures.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

The Teachers shall choose the types of assignments depending on the requirement of the course and plan to attain the Cos and POs. (to have a less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course). CIE methods /test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Three Tests each of 20 Marks;

- 1st, 2nd, and 3rd tests shall be conducted after completion of the syllabus of 30-35%, 70-75%, and 90-100% of the course/s respectively.
- Assignments/Seminar/quiz/group discussion /field survey & report presentation/ course project/Skill development activities, suitably planned to attain the COs and POs for a total of 40 Marks.

If the nature of the courses requires assignments/Seminars/Quizzes/group discussion two evaluation components shall be conducted. If course project/field survey/skill development activities etc then the evaluation method shall be one.

Total CIE marks (out of 100 marks) shall be scaled down to 50 marks

Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English/Kannada). The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks. The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks.**
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:**Books (Title of the Book/Name of the author/Name of the publisher/Edition and Year)****Text Books:**

1. Basic Electrical Engineering by D C Kulshreshtha, Tata McGraw Hill, First Edition 2019.
2. A text book of Electrical Technology by B.L. Theraja, S Chand and Company, reprint edition 2014.

Reference Books:

1. Basic Electrical Engineering, D. P. Kothari and I. J. Nagrath, Tata McGraw Hill 4th edition, 2019.
2. Principles of Electrical Engineering & Electronics by V. K. Mehta, Rohit Mehta, S. Chand and Company Publications, 2nd edition, 2015.
3. Electrical Technology by E. Hughes, Pearson, 12th Edition, 2016.
4. Electrical and electronic measurements and instrumentation by A K Sawhney, Dhanapat Rai and Co. edition, January 2015

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Wherever required, faculty shall demonstrate the concepts through laboratory experiments.

COs and POs Mapping (Individual teacher has to fill up)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	0	1	1	1	1	0	0	0	1
CO2	3	3	2	1	1	1	0	0	0	0	0	1
CO3	3	2	1	1	1	1	1	1	0	0	0	1
CO4	3	2	2	1	0	1	1	1	0	0	0	1
CO5	3	1	2	0	1	2	1	1	0	0	1	1

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

Course Title:	Basic Electronics (For ECE and Allied Branches)		
Course Code:	BBEE103/203	CIE Marks	50
Course Type (Theory/Practical /Integrated)	Theory	SEE Marks	50
		Total Marks	100
Teaching Hours/Week (L:T:P: S)	3:0:0:0	Exam Hours	03
Total Hours of Pedagogy	40 hours	Credits	03
Course objectives: Students will be taught • Operation of Semiconductor diode, Zener diode and Special purpose diodes and their applications. • Biasing circuits for transistor (BJT) as an amplifier. • Study of linear Op-amps and its applications. • Logic circuits and their optimization. • Principles of Transducers and Communication.			
Teaching-Learning Process These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes and make Teaching –Learning more effective 1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes. 2. Show Video/animation films to explain the functioning of various analog and digital circuits. 3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it. 4. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 5. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1 (8 Hours)			
Semiconductor Diodes: Introduction, PN Junction diode, Characteristics and Parameters, Diode Approximations, DC Load Line analysis (Text 1: 2.1,2.2,2.3,2.4) Diode Applications: Introduction, Half Wave Rectification, Full Wave Rectification, Full Wave Rectifier Power Supply: Capacitor Filter Circuit, RC π Filter (includes numerical) (Text 1: 3.1,3.2,3.4,3.5) Zener Diodes: Junction Breakdown, Circuit Symbol and Package, Characteristics and Parameters, Equivalent Circuit, Zener Diode Voltage Regulator. (Text1:2.9, 3.7)			
Module-2(8 Hours)			
Bipolar Junction Transistors: Introduction BJT Voltages & Currents, BJT Amplification, Common Base Characteristics, Common Emitter Characteristics, Common Collector Characteristics, BJT Biasing: Introduction, DC Load line and Bias point (Text 1: 4.2, 4.3, 4.5,4.6, 5.1) Field Effect Transistor: Junction Field Effect Transistor, JFET Characteristics, MOSFETs: Enhancement MOSFETs, Depletion Enhancement MOSFETs (Text 1: 9.1,9.2,9.5)			
Module-3(8 Hours)			
Operational Amplifiers: Introduction, The Operational Amplifier, Block Diagram Representation of Typical Op-Amp, Schematic Symbol, Op-Amp parameters - Gain, input resistance, Output resistance, CMRR, Slew rate, Bandwidth, input offset voltage, Input bias Current and Input offset Current, The Ideal Op-Amp , Equivalent Circuit of Op-Amp, Open Loop Op-Amp configurations, Differential Amplifier, Inverting & Non Inverting Amplifier Op-Amp Applications: Inverting Configuration, Non-Inverting Configuration, Differential Configuration, Voltage Follower, Integrator, Differentiator (Text 2: 1.1, 1.2, 1.3, 1.5, 2.2, 2.3, 2.4, 2.6, 6.5.1, 6.5.2, 6.5.3, 6.12, 6.13).			
Module-4(8 Hours)			

Boolean Algebra and Logic Circuits: Binary numbers, Number Base Conversion, octal & Hexa Decimal Numbers, Complements, Basic definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Other Logic Operations, Digital Logic Gates (Text 3: 1.2, 1.3, 1.4, 1.5, 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7)

Combinational logic: Introduction, Design procedure, Adders- Half adder, Full adder (Text 3: 4.1, 4.2, 4.3)

Module-5(8 Hours)

Introduction to Transducers: Introduction, Resistive Transducers, Inductive Transducers, Capacitive Transducers, Thermal transducers, Optoelectronic transducer, and Piezoelectric transducers (Text 4: Chapter 18: 18.1, 18.2, 18.3, 18.4, 18.5)

Communications: Introduction to communication, Communication System, Modulation (Text book 5: 1.1, 1.2, 1.3)

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

CO1: Develop the basic knowledge on construction, operation and characteristics of semiconductor devices. (Level: C3)

CO2: Apply the acquired knowledge to construct small scale circuits consisting of semiconductor devices (Level: C3)

CO3: Develop competence knowledge to construct basic digital circuit by make use of basic gate and its function. (Level: C3)

CO4: Construct the conceptual blocks for basic communication system. (Level: C3)

CO5: Apply the knowledge of various transducers principle in sensor system. (Level: C3)

A. CO v/s PO Mapping Table

Cos/POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	-	2	2						
CO2	3	2	3	-	2	1						
CO3	3	2	3	-	3				1			
CO4	2	1	1	-	2	1			1			1
CO5	2	1	1	-	2	1			1			1

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation(CIE):

Three Tests each of 20 Marks;

- 1st, 2nd, and 3rd tests shall be conducted after completion of the syllabus of 30-35%, 70-75%, and 90-100% of the course/s respectively.
- Assignments/Seminar/quiz/group discussion /field survey & report presentation/ course project/Skill development activities, suitably planned to attain the COs and POs for a total of 40 Marks.

If the nature of the courses requires assignments/Seminars/Quizzes/group discussion two evaluation components shall be conducted. If course project/field survey/skill development activities etc then the evaluation method shall be one.

Total CIE marks (out of 100 marks) shall be scaled down to 50 marks

Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English). The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks. The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks**.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:**Books (Title of the Book/Name of the author/Name of the publisher/Edition and Year)**

1. Electronic Devices and Circuits, David A Bell, 5th Edition, Oxford, 2016
2. Op-amps and Linear Integrated Circuits, Ramakanth A Gayakwad, Pearson Education, 4th Edition
3. Digital Logic and Computer Design, M. Morris Mano, PHI Learning, 2008 ISBN-978-81-203-0417-8
4. Electronic Instrumentation and Measurements (3rd Edition) – David A. Bell, Oxford University Press, 2013
5. Electronic Communication Systems, George Kennedy, 4th Edition, TMH

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/courses/122106025>
- <https://nptel.ac.in/courses/108105132>
- <https://nptel.ac.in/courses/117104072>

16-2-2022

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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**VISVESVARAYA TECHNOLOGICAL
UNIVERSITY, BELAGAVI**

**B.E: Electronics & Communication
Engineering / B.E: Electronics &
Telecommunication Engineering
NEP, Outcome Based Education
(OBE) and Choice Based Credit
System (CBCS)**

**Syllabus for BE III Semester 2022
Scheme
w.e.f 2023-24**

AV Mathematics-III for EC Engineering		Semester	3
Course Code	BMATEC301	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:1:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
Course objectives: • Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis and to enable the student to express non-periodic functions to periodic functions using the Fourier series and Fourier transforms. • Analyze signals in terms of Fourier transforms • Develop the knowledge of solving differential equations and their applications in Electronics & Communication engineering. • To find the association between attributes and the correlation between two variables			
Teaching-Learning Process			
Pedagogy (General Instructions): These are sample Strategies, teachers can use to accelerate the attainment of the various course outcomes. 1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills. 2. State the need for Mathematics with Engineering Studies and Provide real-life examples. 3. Support and guide the students for self-study. 4. You will assign homework, grading assignments and quizzes, and documenting students' progress. 5. Encourage the students to group learning to improve their creative and analytical skills. 6. Show short related video lectures in the following ways: • As an introduction to new topics (pre-lecture activity). • As a revision of topics (post-lecture activity). • As additional examples (post-lecture activity). • As an additional material of challenging topics (pre-and post-lecture activity). • As a model solution of some exercises (post-lecture activity).			
Module-1: Fourier series and practical harmonic analysis			
Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period 2π and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis, variation of periodic current.(8 hours) (RBT Levels: L1, L2 and L3)			
Module-2: Infinite Fourier Transforms			
Infinite Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms, discrete Fourier transform (DFT), Fast Fourier transform (FFT). (8 hours) (RBT Levels: L1, L2 and L3)			
Module-3: Z Transforms			

Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity, scaling, first and second shifting, multiplication by n. Initial and final value theorem. Inverse Z- transforms. Application to difference equations. (8 hours) (RBT Levels: L1, L2 and L3)
Module-4: Ordinary Differential Equations of Higher Order
Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems. Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations-Problems. Application of linear differential equations to L-C circuit and L-C-R circuit. (8 hours) (RBT Levels: L1, L2 and L3)
Module-5: Curve fitting, Correlation, and Regressions
Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$, $y = a + bx + cx^2$, and $y = ax^b$. Correlation, Coefficient of correlation, Lines of regression, Angle between regression lines, standard error of estimate, rank correlation. (RBT Levels: L1, L2 and L3)(8 hours)
Course outcome (Course Skill Set) At the end of the course, the student will be able to: 1. Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing, and field theory. 2. To use Fourier transforms to analyze problems involving continuous-time signals 3. To apply Z-Transform techniques to solve difference equations 4. Understand that physical systems can be described by differential equations and solve such equations 5. Make use of correlation and regression analysis to fit a suitable mathematical model for statistical data

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:**Books (Name of the author/Title of the Book/Name of the publisher/Edition and Year)****Text Books:**

1. **B. S. Grewal:** “Higher Engineering Mathematics”, Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig:** “Advanced Engineering Mathematics”, John Wiley & Sons, 10thEd., 2018.

Reference Books:

1. **V. Ramana:** “Higher Engineering Mathematics” McGraw-Hill Education, 11thEd., 2017
2. **Srimanta Pal & Subodh C.Bhunia:** “Engineering Mathematics” Oxford University Press, 3rdEd., 2016.
3. **N.P Bali and Manish Goyal:** “A Textbook of Engineering Mathematics” Laxmi Publications, 10thEd., 2022.
4. **C. Ray Wylie, Louis C. Barrett:** “Advanced Engineering Mathematics” McGraw–Hill Book Co., New York, 6thEd., 2017.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** “Engineering Mathematic for Semester I and II”, McGraw Hill Education(India) Pvt. Ltd 2015.
6. **H.K. Dass and Er. Rajnish Verma:** “Higher Engineering Mathematics” S.Chand Publication, 3rdEd.,2014.
7. **James Stewart:** “Calculus” Cengage Publications, 7thEd., 2019.

Web links and Video Lectures (e-Resources):

- <http://nptel.ac.in/courses.php?disciplineID=111>
- [http://www.class-central.com/subject/math\(MOOCs\)](http://www.class-central.com/subject/math(MOOCs))
- <http://academicearth.org/>
- VTU e-Shikshana Program
- VTU EDUSAT Program.

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Quizzes
- Assignments
- Seminar

Digital System Design using Verilog		Semester	3
Course Code	BEC302	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory/Practical		
Course objectives: This course will enable students to: • To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques. • To impart the concepts of designing and analyzing combinational logic circuits. • To impart design methods and analysis of sequential logic circuits. • To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing. • Encourage collaborative (Group) Learning in the class. • Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes. • Give Programming Assignments.			
MODULE-1			
Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms.(Section3.1to3.5ofText1).			
MODULE-2			
Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices(PLDs) (Section5.1to5.7 ofText2)			
MODULE-3			

Flip-Flops and its Applications: The Master-Slave Flip-flops(Pulse-Triggered flip-flops):SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops.(Section 6.4, 6.6 to 6.9 (Excluding 6.9.3)of Text2)

MODULE-4

Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section1.1to1.6.2, 1.6.4 (only Verilog),2 of Text 3)

Verilog Data flow description: Highlights of Data flow description, Structure of Data flow description.(Section2.1to2.2(only Verilog) of Text3)

MODULE-5

Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (onlyVerilog)of Text 3)

Verilog Structural description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section4.1 to 4.2 of Text 3)

PRACTICAL COMPONENT OF IPCC (Experiments can be conducted either using any circuit simulation software or discrete components)

Sl.N	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor(Full/half)circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description:1:8Demux, 3:8 decoder,2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d)D type
8	To realize Counters-up/down (BCD and binary)using Verilog Behavioral description.
Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.
Course outcomes (Course Skill Set): At the end of the course the student will be able to: 1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique. 2. Analyze and design for combinational logic circuits. 3. Analyze the concepts of Flip Flops(SR, D,T and JK) and to design the synchronous sequential circuits using Flip Flops. 4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.	

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-

questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Digital Logic Applications and Design by John MYarbrough, Thomson Learning, 2001.
2. Digital Principles and Design by Donald DGivone, McGrawHill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream techpress.

ReferenceBooks:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
3. Fundamentals of HDL, by Cyril PR, Pearson/Sanguine 2010

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments/Mini Projects can be given to improve programming skills.

Electronic Principles and Circuits		Semester	3
Course Code	BEC303	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	
Examination nature (SEE)	Theory/Practical		
Course objectives: This course will enable students to • Design and analyse the BJT circuits as an amplifier and voltage regulation. • Design of MOSFET Amplifiers and analyse the basic amplifier configurations using small signal equivalent circuit models • Design of operational amplifiers circuits as Comparators, DAC and filters. • Understand the concept of positive and negative feedback. • Analyze Power amplifier circuits in different modes of operation. • Construct Feedback and Oscillator circuits using FET. • Understand the thyristor operation and the different types of thyristors.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. 1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. 2. Show Video/animation films to explain evolution of communication technologies. 3. Encourage collaborative (Group) Learning in the class 4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking 5. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. 6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
MODULE-1			
BJT AC models: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier. Voltage Amplifiers: Voltage gain, Multistage Amplifiers. CC and CB Amplifiers: CC Amplifier, Output Impedance, Cascading CE and CC, Darlington Connections, Voltage regulation, The Common base Amplifier. [Text1]			
MODULE-2			

MOSFET

Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower.

MODULE-3

Linear Opamp Circuits: Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis.

Oscillator: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.

The 555 timer: Monostable Operation, Astable Operation.

[Text1]

MODULE-4

Negative Feedback: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).

Active Filters: Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters.

[Text1]

MODULE-5

Power Amplifiers: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation.

Thyristors: The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors.

[Text1]

PRACTICAL COMPONENT OF IPCC (Experiments can be conducted either using any circuit simulation software or discrete components)

Sl.NO	Experiments
1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator
2	Design and Test Biased Clippers – a) Positive, b) Negative, c) Positive-Negative Positive and Negative Clampers with and without Reference.
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
5	Design and test (i) Emitter Follower, (ii) Darlington Connection
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier
7	Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve.
8	Design and test Full wave Controlled rectifier using RC triggering circuit.
9	Design and test Precision Half wave and full wave rectifiers using Opamp
10	Design and test RC phase shift oscillator

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
- Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
- Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
- Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
- Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods

mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

5. The question paper will have ten questions. Each question is set for 20 marks.
6. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
7. The students have to answer 5 full questions, selecting one full question from each module.
8. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:**Books**

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015. ISBN:978-0-19-808913-1

Web links and Video Lectures (e-Resources):

1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Network Analysis		Semester	3
Course Code	BEC304	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: 1. Apply mesh and nodal techniques to solve an electrical network. 2. Solve different problems related to Electrical circuits using Network Theorems and Two port network. 3. Familiarize with the use of Laplace transforms to solve network problems. 4. Study two port network parameters and their applications. 5. Study of RLC Series and parallel tuned circuit.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Encourage collaborative (Group) Learning in the class. • Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.			
Module-1			
Basic Concepts: Practical sources, Source transformations, Network reduction using Star - Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.			
Module-2			
Network Theorems: Superposition, Millman's theorems, Thevenin's and Norton's theorems, Maximum Power transfer theorem.			
Module-3			
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and			

RLC circuits for AC and DC excitations.
Module-4
Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.
Module-5
Two port network parameters: Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets. Resonance: Series Resonance: Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance. Parallel Resonance: Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Determine currents and voltages using source transformation/ source shifting/ mesh/ nodal analysis and reduce given network using star- delta transformation. 2. Solve problems by applying Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions. 3. Analyse the circuit parameters during switching transients and apply Laplace transform to solve the given network 4. Evaluate the frequency response for resonant circuits and the network parameters for two port networks

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

9. The question paper will have ten questions. Each question is set for 20 marks.

10. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:**Books**

1. M.E.Van Valkenburg (2000), Network Analysis, Prentice Hall of India, 3rd edition, 2000, ISBN:9780136110958.
2. Roy Choudhury-Networks and Systems, 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677

ReferenceBooks:

3. Hayt, Kemmerly and Durbin-Engineering Circuit Analysis, **TMH**7th Edition, 2010.
4. J.David Irwin/ R.Mark Nelms- Basic Engineering Circuit Analysis JohnWiley,8thed,2006.
5. Charles K Alexander and Mathew NO Sadiku-Fundamentals of Electric Circuits, Tata

McGraw-Hill, 3rd Ed, 2009.
Web links and Video Lectures (e-Resources):
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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
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Analog and Digital Systems Design Laboratory		Semester	3
Course Code	BECL305	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	Practical		
Course objectives: This laboratory course enables students to • Understand the electronic circuit schematic and its working • Realize and test amplifier and oscillator circuits for the given specifications • Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers. • Study the static characteristics of SCR and test the RC triggering circuit. • Design and test the combinational and sequential logic circuits for their functionalities. • Use the suitable ICs based on the specifications and functions.			
Sl.NO	Experiments (<i>All the experiments has to be conducted using discrete components</i>)		
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain-bandwidth product, input and output impedances.		
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator		
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator		
4	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16		
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor& Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).		
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa		
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.		
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192		
	Demonstration Experiments (For CIE)		
9	Design and Test the second order Active Filters and plot the frequency response, i) Low pass Filter ii) High pass Filter		
10	Design and test the following using 555 timer i) MonostableMultivibraator ii) AstableMultivibrator		
11	Design and Test a Regulated Power supply		
12	Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.		

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic circuit experiments using 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled

down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual", 5th Edition, 2009, Oxford University Press.
2. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, McGraw Hill Education, 2017.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

Electronic Devices		Semester	3
Course Code	BEC306A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: • Understand the basics of semiconductor physics and electronic devices. • Describe the mathematical models BJTs and FETs along with the constructional details. • Understand the construction and working principles of optoelectronic devices • Understand the fabrication process of semiconductor devices and CMOS process integration.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method(L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Encourage collaborative(Group)Learning in the class. • Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the realworld-and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.			
Module-1			
Semiconductors Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. (Text1:3.1.1,3.1.2,3.1.3,3.1.4,3.2.1,3.2.3,3.2.4,3.4.1,3.4.2,3.4.3,3.4.5).			
Module-2			
PN Junctions Forward and Reverse biased junctions-Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers.(Text1:5.3.1,5.3.3,5.4.1,5.4.2,5.4.3) Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials. (Text1:8.1.1,8.1.2,8.1.3,8.2,8.2.1),			
Module-3			

Bipolar Junction Transistor

Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupled Diode model(Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown.

(Text1:7.1,7.2,7.3,7.5.1,7.6,7.7.1,7.7.2, 7.7.3)

Module-4**Field Effect Transistors**

Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET-Two terminal MO Sstructure- Energy band diagram, Ideal Capacitance
-Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics.

(Text2:9.1.1,9.4,9.6.1,9.6.2,9.7.1,9.7.2,9.8.1,9.8.2).

Module-5**Fabrication of p-n junctions**

Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. (Text 1: 5.1)

Integrated Circuits

Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements.(Text 1:9.1,9.2,9.3.1,9.3.3).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the principles of semiconductor Physics
2. Understand the principles and characteristics of different types of semiconductor devices
3. Understand the fabrication process of semiconductor devices
4. Utilize the mathematical models of semiconductor junctions for circuits and systems.
5. Identify the mathematical models of MOS transistors for circuits and systems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

13. The question paper will have ten questions. Each question is set for 20 marks.
14. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
15. The students have to answer 5 full questions, selecting one full question from each module.
16. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

6. Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices", 7th Edition, Pearson Education, 2016, ISBN 978-93-325-5508-2.
7. Donald A Neamen, Dhruves Biswas, "Semiconductor Physics and Devices", 4th Edition, McGraw Hill Education, 2012, ISBN 978-0-07- 107010-2.

Reference Books:

8. S.M.Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3rd Edition, Wiley, 2018.
9. Adir Bar-Lev, "Semiconductor and Electronic Devices", 3rd Edition, PHI, 1993

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

Sensors and Instrumentation		Semester	3
Course Code	BEC306B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: • Understand various technologies associated in manufacturing of sensors • Acquire knowledge about types of sensors used in modern digital systems • Get acquainted about material properties required to make sensors • Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters. • Describe principle of operation of digital measuring instruments and Bridges. • Understand the operations of transducers and instrumentation amplifiers.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method(L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Encourage collaborative(Group)Learning in the class. • Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the realworld-and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.			
Module-1			
Introduction to sensor based measurement systems: General concepts and terminology, sensor classification, Primary Sensors, material for sensors, microsensor technology. (Text 1)			
Module-2			
Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors. (Text 1)			
Module-3			
Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error.(Text 2: 1.2-1.6) Multirange Ammeters, Multirange voltmeter.(Text2:3.2,4.4) Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM (Text 2: 5.1-5.3, 5.5,5.6)			
Module-4			
Digital Multimeter: Digital Frequency Meter and Digital Measurement of Time, Function Generator. Bridges: Measurement of resistance: Wheatstone's Bridge, AC Bridges - Capacitance and Inductance Comparison bridge, Wien's bridge.			

(Text2:refer 6.2,6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8, 11.2, 11.8 -11.10, 11.14).

Module-5

Transducers: Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT.

(Text2:13.1-13.3,13.5, 13.6 up to 13.6.1,13.7,13.8,13.11).

Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Analog Weight Scale(Text2:14.3.3, 14.4.1, 14.4.3).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

5. Understand the material properties required to make sensors
6. Understand the principle of transducers for measuring physical parameters.
7. Describe the manufacturing process of sensors
8. Analyze the instrument characteristics and errors.
9. Describe the principle of operation and develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

17. The question paper will have ten questions. Each question is set for 20 marks.
18. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
19. The students have to answer 5 full questions, selecting one full question from each module.
20. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:**Books**

1. "Sensors and Signal Conditioning", Ramon Pallas Areny, JohnG. Webster, 2nd edition, John Wiley and Sons, 2000
2. H.S.Kalsi, "Electronic Instrumentation", Mc Graw Hill, 3rd Edition, 2012, ISBN: 9780070702066.

Reference Books

1. David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN 81-203-2360-2.
2. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015, ISBN: 9789332556065.

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Computer Organization and Architecture		Semester	3
Course Code	BEC306C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: This course will enable students to:			
• Explain the basic sub systems of a computer, their organization, structure and operation. • Illustrate the concept of programs as sequences of machine instructions. • Demonstrate different ways of communicating with I/O devices • Describe memory hierarchy and concept of virtual memory. • Illustrate organization of simple pipelined processor and other computing systems.			
Teaching-Learning Process (General Instructions)			
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.			
These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.			
• Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Encourage collaborative (Group) Learning in the class. • Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.			
Module-1			
Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance -Processor Clock, Basic Performance Equation(upto1.6.2ofChap1ofText).			
Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing (up to 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).			
Module-2			

Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions (from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of Text).
Module-3
Input/ Output Organization: Accessing I/O Devices, Interrupts -Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access (upto 4.2.4 and 4.4 except 4.4.1 of Chap 4 of Text).
Module-4
Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage- Magnetic Hard Disks (5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).
Module-5
Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control (up to 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Explain the basic organization of a computer system. 2. Describe the addressing modes, instruction formats and program control statement. 3. Explain different ways of accessing an input/ output device including interrupts. 4. Illustrate the organization of different types of semiconductor and other secondary storage memories. 5. Illustrate simple processor organization based on hard wired control and micro-programmed control.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

21. The question paper will have ten questions. Each question is set for 20 marks.

22. There will be 2 questions from each module. Each of the two questions under a module (with

Suggested Learning Resources:**Book**

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGrawHill, 2002.

ReferenceBooks:

2. David A. Patterson, John L. Hennessy: Computer Organization and Design-The Hardware/ Software Interface ARM Edition, 4th Edition, Elsevier, 2009.
3. William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.
4. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

Web links and Video Lectures (e-Resources):
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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
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Applied Numerical Methods for EC Engineers		Semester	3
Course Code	BEC306D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
Course objectives: • To provide the knowledge and importance of error analysis in engineering problems • To represent and solve an application problem using a system of linear equations • Analyzeregression data to choose the most appropriate model for a situation. • Familiarize with the ways of solving complicated mathematical problems numerically • Prepare to solve mathematical models represented by initial or boundary value problems			
Teaching-Learning Process			
Pedagogy (General Instructions): These are sample Strategies, teachers can use to accelerate the attainment of the various course outcomes. 1. In addition to the traditional lecture method, different innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills. 2. State the need for Mathematics with Engineering Studies and Provide real-life examples. 3. Support and guide the students for self-study. 4. You will assign homework, grading assignments and quizzes, and documenting students' progress. 5. Encourage the students to group learning to improve their creative and analytical skills. 6. Show short related video lectures in the following ways: • As an introduction to new topics (pre-lecture activity). • As a revision of topics (post-lecture activity). • As additional examples (post-lecture activity). • As an additional material of challenging topics (pre-and post-lecture activity). • As a model solution of some exercises (post-lecture activity).			
Module-1: Errors in computations and Root of the equations			
Approximations and Round Off -Errors in computation: Error definitions, Round-Offerrors, Truncation errors and the Taylor series-The Taylor series, Error Propagation, Total numerical error,Absolute,Relative and percentage errors,Blunders, Formulation errors and data uncertainty. Roots of equations: Simple fixed point iteration methods. Secant Method, Muller's method, and Graeffe's Roots Squaring Method. Aitkin's Method. (8 hours) (RBT Levels: L1, L2 and L3)			
Module-2: Solution of System of Linear Equations			
Rank of the matrix, Echelon form, Linearly dependent and independent equations, Solutions for linear equations, Partition method, Croute's Triangularisation method. Relaxation method. Solution of non-linear simultaneous equations by Newton-Raphson method. Eigen Values and properties, Eigen Vectors, Bounds on Eigen Values, Jacobi's method, Given's method for symmetric matrices. (8 hours) (RBT Levels: L1, L2 L3)			

Module-3: Curve Fitting
Least-Squares Regression: Linear Regressions, Polynomial regressions, Multiple Linear regressions, General Linear Least squares, Nonlinear Regressions, QR Factorization. Curve Fitting with Sinusoidal Functions Introduction to Splines, Linear Splines, Quadratic Splines, Cubic Splines. Bilinear Interpolation. (8 hours) (RBT Levels: L1, L2 L3)
Module-4: Numerical integration, Difference equations and Boundary Value Problems
Romberg's method, Euler-Maclaurin formula, Gaussian integration for $n = 2$ and $n=3$. Numerical double integration by trapezoidal and Simpson's 1/3 rd rule. Solution of linear difference equations. Boundary-Value Problems, Introduction. The Shooting Method, Finite-Difference Methods (8 hours) (RBT Levels: L1, L2 and L3)
Module-5: Numerical solution of partial differential equations
Classifications of second-order partial differential equations, Finite difference approximations to partial derivatives. Solution of: Laplace equation, Poisson equations, one-dimensional heat equation and wave equations. (8 hours) (RBT Levels: L1, L2 and L3)
Course outcome (Course Skill Set) At the end of the course, the student will be able to: 1. Explain and measure errors in numerical computations 2. Test for consistency and solve a system of linear equations. 3. Construct a function which closely fits given n- n-points of an unknown function. 4. Understand and apply the basic concepts related to solving problems by numerical differentiation and numerical integration. 5. Use appropriate numerical methods to study phenomena modelled as partial differential equations.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE, the minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

5. The question paper will have ten questions. Each question is set for 20 marks.
6. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
7. The students have to answer 5 full questions, selecting one full question from each module.
8. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books (Name of the author/Title of the Book/Name of the publisher/Edition and Year)

Text Books:

1. **Steven C. Chapra & Raymond P. Canale:** "Numerical Methods for Engineers and Scientists", McGraw Hill, 8th Edition, 2020.
2. **Steven C. Chapra:** "Applied Numerical Methods with MATLAB for Engineers and Scientists", McGraw Hill, Fifth Edition, 2023.
3. **B. S. Grewal:** "Numerical Methods in Engineering & Science with programs in C, C++ and MATLAB", Khanna Publishers, 10th Ed., 2015.

Reference Books:

1. **John H. Mathews & Kurtis D. Frank:** "Numerical Methods Using MATLAB", PHI Publications, 4th Edition, 2005.
2. **Won Young Yang, Wenwu Cao, Tae Sang Chung, John Morris:** "Applied Numerical Methods Using MATLAB", WILEY Interscience, Latest Edition, 2005.

Web links and Video Lectures (e-Resources):

- <http://nptel.ac.in/courses.php?disciplineID=111>
- [http://www.class-central.com/subject/math\(MOOCs\)](http://www.class-central.com/subject/math(MOOCs))
- <http://academicearth.org/>
- VTU e-Shikshana Program
- VTU EDUSAT Program.

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Quizzes
- Assignments
- Seminar

LabVIEW Programming		Semester	3
Course Code	BEC358A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	Practical		
Course objectives: • Aware of various front panel controls and indicators. • Connect and manipulate nodes and wires in the block diagram. • Locate various tool bars and pull-down menus for the purpose of implementing specific functions. • Locate and utilize the context help window. • Familiar with LabVIEW and different applications using it.			
Sl.NO	VI Programs(using LabVIEW software)to realize the following:		
1	Basic arithmetic operations: addition, subtraction, multiplication and division		
2	Boolean operations: AND, OR, XOR, NOT and NAND		
3	Sum of ‘n’ numbers using ‘for’ loop		
4	Factorial of a given number using ‘for’ loop		
5	Determine square of a given number		
6	Factorial of a given number using ‘while’ loop		
7	Sorting even numbers using ‘while’ loop in an array		
8	Finding the array maximum and array minimum		
	Demonstration Experiments (For CIE)		
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.		
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).		
11	Build a Virtual Instrument that simulates a Water Level Detector.		
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.		
Course outcomes (Course Skill Set): At the end of the course the student will be able to: • Use LabVIEW to create data acquisition, analysis and display operations • Create user interfaces with charts, graph and buttons • Use the programming structures and data types that exist in LabVIEW • Use various editing and debugging techniques.			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. VirtualInstrumentationusingLABVIEW,JovithaJerome,PHI,2011
2. VirtualInstrumentationusingLABVIEW, SanjayGupta, JosephJohn, TMH, McGrawHill, SecondEdition, 2011.

MATLAB Programming		Semester	3
Course Code	BEC358B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0	SEE Marks	50
Total Hours of Pedagogy	14	Total Marks	100
Credits	01	Exam Hours	
Examination type (SEE)	Theory		
Course objectives: • Understand the MATLAB commands and functions. • Create and Execute the script and function files • Work with built in function, saving and loading data and create plots. • Work with the arrays, matrices, symbolic computations, files and directories. • Learn MATLAB programming with script, functions and language specific features.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Adopt Problem Based Learning (PBL), which fosters students’ analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. 2. Give programming assignments.			
Module-1			
Introduction: Basics of MATLAB, Simple arithmetic calculations, Creating and working with arrays and numbers.			
Module-2			
Creating and printing simple plots, Creating, saving and executing a script file, Creating and executing a function file, Working with arrays and matrices.			
Module-3			
Working with anonymous functions, Symbolic Computations, Importing and exporting data, Working with files and directories.			
Module-4			
Interactive computations: Matrices and vectors, Matrix and array operations, Character strings, Command line functions, Built-in functions, Saving and loading data, Plotting simple plots.			
Module-5			
Programming in MATLAB: Script Files, Function Files, Language specific Features.			
Course outcome (Course Skill Set) At the end of the course the student will be able to: 10. Understand the syntax of MATLAB for arithmetic computations, arrays, matrices. 11. Understand the built in function, saving and loading data, and create plots 12. Create program using symbolic computations, Importing and exporting data and files 13. Create program using character strings, Command line functions and Built-in functions.			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour**. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

OR

MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then

25. The question paper will have ten questions. Each question is set for 10 marks.
26. There will be 2 questions from each module. Each of the two questions under a module may or may not have the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).
27. The students have to answer 5 full questions, selecting one full question from each module.
- 28. The duration of the examinations shall be defined by the concerned board of studies**

Suggested Learning Resources:**Book**

3. Rudra Pratap, Getting Started with MATLAB – A quick Introduction for scientists and Engineers, Oxford University Press, 2010.

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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C++ Basics		Semester	4
Course Code	BEC358C	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Total Hours of Pedagogy	24	Total Marks	100
Credits	1	Exam Hours	03
Examination nature (SEE)	Practical		
Course objectives:			
• Understand object-oriented programming concepts, and apply them in solving problems. • To create, debug and run simple C++ programs. • Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading. • Introduce the concepts of exception handling and multithreading.			
Sl.No	Experiments		
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.		
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.		
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.		
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and - operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error		
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: <i>First Name, Surname, DOB & bank Balance</i> and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.		
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.		
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().		
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.		
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).		
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.		
11	Write a C++ program to create three objects for a class named count object with data members		

	such as roll_no & Name. Create a members function set_data () for setting the data values & display () member function to display which object has invoked it using „this“ pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.
Course outcomes (Course Skill Set): At the end of the course the student will be able to: 1. Write C++ program to solve simple and complex problems 2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems. 3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set. 4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE). Continuous Internal Evaluation (CIE): CIE marks for the practical course is 50 Marks . The split-up of CIE marks for record/ journal and test are in the ratio 60:40 . • Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session. • Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks. • Total marks scored by the students are scaled down to 30 marks (60% of maximum marks). • Weightage to be given for neatness and submission of record/write-up on time. • Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester. • In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce. • The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book • The average of 02 tests is scaled down to 20 marks (40% of the maximum marks). The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.	
Semester End Evaluation (SEE): SEE marks for the practical course is 50 Marks. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University All laboratory experiments are to be included for practical examination. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners. Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and	

result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

IoT for Smart Infrastructure		Semester	3
Course Code	BEC358D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	14	Total Marks	100
Credits	01	Exam Hours	
Examination type (SEE)	Theory/Practical		
Course objectives:			
□ To provide an understanding of the concepts, principles, and applications of IoT in the context of smart infrastructure. □ To explore the role of IoT technologies in transforming infrastructure into smart, efficient, and sustainable systems and analyse the challenges, opportunities, and considerations in implementing IoT for smart infrastructure. □ To examine real-world case studies and successful implementations of IoT in smart cities, buildings, transportation, and energy management and explore future trends and emerging technologies shaping the field of IoT for smart infrastructure.			

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

- **Interactive Lectures:** Conduct interactive lectures to present the theoretical concepts and foundational knowledge of IoT for smart infrastructure.
- **Case Studies and Group Discussions:** Utilize case studies to analyse real-world implementations of IoT in smart infrastructure projects. Divide students into groups and assign them specific cases to discuss and analyse.
- **Hands-on Workshops and Simulations:** Organize hands-on workshops or simulations where students can interact with IoT devices and technologies relevant to smart infrastructure.
- **Guest Lectures and Industry Experts:** Invite guest speakers or industry experts who have hands-on experience in implementing IoT in smart infrastructure projects. They can share their insights, challenges, and success stories, providing students with a real-world perspective.
- **Project-Based Learning:** Assign students to work on individual or group projects related to IoT for smart infrastructure. Provide a project brief with specific objectives and deliverables. Students can apply their knowledge and skills to design, develop, or analyse IoT solutions for smart infrastructure challenges.

Module-1

Introduction to IoT and Smart Infrastructure

Introduction to IoT: Definition of IoT and its basic components, Overview of IoT applications in various industries, Importance of IoT in transforming infrastructure.

Smart Infrastructure Overview: Introduction to smart infrastructure and its key components, Benefits and challenges of implementing smart infrastructure, Case studies showcasing successful smart infrastructure projects.

IoT Technologies for Smart Infrastructure: Sensors and actuators: Types, functionalities, and applications; Communication protocols: Wi-Fi, Bluetooth, cellular networks, and their use in IoT;

Cloud computing and data analytics in IoT for infrastructure; Edge computing: Real-time decision-making at the edge.

Security and Privacy in IoT for Smart Infrastructure: Security challenges and threats in IoT, Privacy considerations and data protection in smart infrastructure, best practices and solutions for ensuring IoT security and privacy.

Module-2

IoT Applications in Smart Cities

Introduction to Smart Cities - Definition and key features of smart cities, Role of IoT in transforming cities into smart cities, Benefits and challenges of smart city implementations.

IoT Applications in Smart City Infrastructure - Smart transportation: Intelligent traffic management and transportation systems, Smart buildings: Energy management and occupant comfort; Smart grids: Optimizing energy distribution and consumption; Waste management, water management, and environmental monitoring.

Case Studies of Smart City Implementations: Showcase of successful smart city projects around the world; Analysis of the IoT technologies and strategies implemented; Lessons learned from these case studies.

Future Trends in Smart Cities: Emerging technologies shaping the future of smart cities, Role of IoT, AI, and 5G in advancing smart city infrastructure, Opportunities and challenges for future smart city developments.

Module-3

IoT Applications in Smart Buildings

Introduction to Smart Buildings: Definition and key features of smart buildings, Benefits of IoT in improving energy efficiency and occupant comfort, Challenges and considerations in implementing smart building technologies.

IoT Technologies for Smart Buildings: Building automation systems and controls; Energy management and monitoring using IoT devices; Indoor environmental quality monitoring and optimization; Smart lighting and HVAC systems.

Case Studies of Smart Building Implementations: Showcase of successful smart building projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies.

Future Trends in Smart Buildings: Emerging technologies for smart buildings; Integration of IoT with AI and machine learning; Potential impact of 5G on smart building applications.

Module-4

IoT Applications in Smart Transportation

Introduction to Smart Transportation: Definition and key features of smart transportation; Role of IoT in intelligent traffic management and transportation systems; Challenges and opportunities in implementing smart transportation solutions.

IoT Technologies for Smart Transportation: Traffic sensors and monitoring systems; Intelligent transportation systems (ITS); Vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communication; Real-time data analysis and predictive analytics.

Case Studies of Smart Transportation Implementations: Showcase of successful smart transportation projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies.

Future Trends in Smart Transportation: Emerging technologies shaping the future of smart transportation; Role of IoT, AI, and autonomous vehicles; Potential impact of 5G on smart transportation applications.

Module-5

IoT for Smart Grids and Energy Management

Introduction to Smart Grids: Definition and key features of smart grids; Role of IoT in optimizing energy distribution and consumption; Benefits and challenges of smart grid implementations. IoT Technologies for Smart Grids: Smart meters and energy monitoring devices; Demand response and load management; Grid optimization and fault detection using IoT; Renewable energy integration and grid stability.

Case Studies of Smart Grid Implementations: Showcase of successful smart grid projects, Analysis of IoT technologies and solutions deployed, Lessons learned from these case studies.

Future Trends in Smart Grids and Energy Management: Emerging technologies for smart grids; Integration of IoT, AI, and blockchain in energy management; Potential impact of 5G on smart grid applications.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

- Define and explain the core concepts and components of IoT and its relevance to smart infrastructure. Identify and evaluate the key technologies and communication protocols used in IoT for smart infrastructure.
- Assess the benefits, challenges, and ethical considerations associated with implementing IoT in smart infrastructure projects and analyse & compare different IoT applications in smart cities, buildings, transportation, and energy management.
- Examine real-world case studies of successful IoT implementations in smart infrastructure and extract lessons learned. Demonstrate an understanding of security and privacy considerations in IoT for smart infrastructure.
- Discuss the impact of emerging technologies, such as artificial intelligence and 5G, on the future of IoT in smart infrastructure. Apply knowledge and critical thinking skills to propose IoT-based solutions for smart infrastructure challenges.
- Work effectively in teams to analyse, design, and present IoT projects related to smart infrastructure and communicate effectively and articulate the potential benefits and limitations of IoT for smart infrastructure.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's

taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour**. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

OR

MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then

1. The question paper will have ten questions. Each question is set for 10 marks.
2. There will be 2 questions from each module. Each of the two questions under a module may or may not have the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

1. MindMatrix.io
2. "Internet of Things (A Hands-on-Approach)" by Arshdeep Bahga and Vijay Madisetti
3. "Building the Internet of Things: Implement New Business Models, Disrupt Competitors, Transform Your Industry" by Maciej Kranz
4. "Smart Cities: Big Data, Civic Hackers, and the Quest for a New Utopia" by Anthony M. Townsend

5. "Internet of Things for Architects: Architecting IoT solutions by implementing sensors, communication infrastructure, edge computing, analytics, and security" by Perry Lea.

Web links and Video Lectures (e-Resources):

- makes.mindmatrix.io

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- **Sensor Deployment and Data Collection:** Organize a hands-on activity where participants work in groups to deploy sensors in a simulated smart infrastructure environment.
- **Smart City Simulation Game:** Develop a simulation game where participants take on different roles representing stakeholders in a smart city.
- **IoT Solution Design Challenge:** Assign participants to design an IoT-based solution for a specific smart infrastructure problem. They can work individually or in teams to identify the problem, propose an IoT solution, outline the required components and technologies, and create a prototype or presentation.
- **Security and Privacy Risk Assessment:** Conduct a group activity where participants analyse the security and privacy risks associated with IoT deployments in smart infrastructure.
- **Field Visit to Smart Infrastructure Project:** Organize a field visit to a smart infrastructure project, such as a smart building, smart city district, or IoT-enabled transportation system.

**VISVESVARAYA TECHNOLOGICAL
UNIVERSITY, BELAGAVI
B.E: Electronics & Communication
Engineering / B.E: Electronics &
Telecommunication Engineering
NEP, Outcome Based Education (OBE)
and Choice Based Credit System
(CBCS)**

**Syllabus for BE IV Semester
2022 Scheme
w.e.f 2023-24**

Engineering Electromagnetics		Semester	4
Course Code	BEC401	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: • Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient. • Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions. • Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions. • Infer the effects of magnetic forces, materials and inductance. • Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media. • Acquire knowledge of Poynting theorem and its application of power flow.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Encourage collaborative (Group) Learning in the class. • Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussion on the topic in the succeeding classes.			
Module-1			
Revision of Vector Calculus-(Text1:Chapter1) Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems.(Text: Chapter 2.1 to 2.5, 3.1)			
Module-2			

Gauss's law and Divergence: Gauss law, Application of Gauss law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell's First equation (Electrostatics), Vector Operator ∇ and divergence theorem, Numerical Problems (**Text: Chapter 3.2 to 3.7**).

Energy, Potential and Conductors: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems (**Text: Chapter 4.1 to 4.4 and 4.6**). Current and Current density, Continuity of current. (**Text: Chapter 5.1, 5.2**)

Module-3

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solution of Laplace's equation, Numerical problems on Laplace equation (**Text: Chapter 7.1 to 7.3**)

Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials, Numerical problems. (**Text: Chapter 8.1 to 8.6**)

Module-4

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems (**Text: Chapter 9.1 to 9.3**).

Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems (**Text: Chapter 9.6 to 9.7**).

Faraday's law of Electromagnetic Induction -Integral form and Point form, Numerical problems (**Text: Chapter 10.1**)

Module-5

Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems (**Text: Chapter 10.2 to 10.4**)

Uniform Plane Wave: Plane wave, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between $\mathbf{E}$ and $\mathbf{H}$, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (y, a, μ , ϵ) and good conductors, Skin effect or Depth of penetration, Poynting's theorem and wave power, Numerical problems. (**Text: Chapter 12.1 to 12.4**)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.
3. Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating

Magnetic field for different current configurations

4. Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
5. Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. W.H.Hayt and J.A. Buck, -Engineering Electromagnetics, 8th Edition, Tata McGraw-Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

2. Elements of Electromagnetics –Matthew N.O., Sadiku, Oxford university press, 4th Edn.
3. Electromagnetic Waves and Radiating systems-E.C. Jordan and K.G. Balmain, **PHI**, 2nd Edn.
4. Electromagnetics-Joseph Edminister, Schaum Outline Series, McGraw Hill.
5. Fundamentals of Electromagnetics for Engineering-N. Narayana Rao, Pearson

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Basic Signal Processing		Semester	4
Course Code	BEC402	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3
Examination nature (SEE)	Theory/practical		
Course objectives: This course will enable students to: Preparation: To prepare students with fundamental knowledge /overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications. Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant(LTI) systems in time and transform domains			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods maybe adopted to develop the outcomes. • Show Video/animationfilmstoexplainthedifferentconceptsofLinearAlgebra&SignalProcessing. • Encourage collaborative (Group)Learning in the class. • Ask at least three HOTS(Higher order Thinking) questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Showthedifferentwaystosolvethesameproblemandencouragethestudentstocomeupwiththeir owncreative ways to solve them. • Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the that topic in the succeeding classes. • Give Programming Assignments.			
MODULE-1			
Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis anddimension,Dimensionsofthefoursubspaces,Rank-NullityTheorem,LinearTransformationsOrthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure (ReferChapters2and3of Text1)			

MODULE-2
Eigen values and Eigen vectors: Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. (Refer Chapter 5, Text 1)
MODULE-3
Introduction and Classification of signals: Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions Basic Operations on signals: Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other wave forms in terms of elementary signals System Classification and properties: Linear-nonlinear, Time variant-invariant, causal-non-causal, static-dynamic, stable-unstable, invertible. (Text 2) [Only for Discrete Signals & Systems]
MODULE-4
Time domain representation of LTI System: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. LTI system Properties in terms of impulse response: System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response (Text 2) [Only for Discrete Signals & Systems]
MODULE-5
The Z-Transforms: Z-transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. (Text 2)

PRACTICAL COMPONENT OF IPCC

Sl.N O	Experiments execute dusing programming languages Scilab / MATLAB (but not limited to)
1	a. Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.
7	Program to generate discrete waveforms.
8	Program to perform asic operation on signals.
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the basics of Linear Algebra
2. Analyze different types of signals and systems
3. Analyze the properties of discrete-time signals & systems
4. Analyse discrete time signals & systems using Z transforms

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests

(Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

5. The question paper will have ten questions. Each question is set for 20 marks.
6. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
7. The students have to answer 5 full questions, selecting one full question from each module.
8. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical

component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51-239-4.

Reference Books

3. Michael Roberts, "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
4. Alan V Oppenheim, Alan S Willsky and S Hamid Nawab, "Signals and Systems" Pearson Education Asia/ PHI, 2nd edition, 1997. Indian Reprint 2002.
5. H P H su, R Ranjan, "Signals and Systems", Schaum's outlines, TMH, 2006.
6. BP Lathi, "Linear Systems and Signals", Oxford University Press, 2005.
7. Ganesh Rao and Satish Tunga, "Signals and Systems", Pearson/Sanguine.
8. Seymour Lipschutz, Marc Lipson, "Schaums Easy Outline of Linear Algebra", 2020.

Web links and Video Lectures (e-Resources):

Videolectures on Signals and Systems by Alan V Oppenheim

[Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube](#)

[Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube](#)

NPTEL videolectures on signals and system:

[https://www.youtube.com/watch?v=7Z3LE5uM-](https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx)

[6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx](https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx) Videolectures on Linear Algebra by Gilbert

Strang

<https://www.youtube.com/watch?v=ZK3O402wflc&list=PL49CF3715CB9EF31D&index=1>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments/Mini Projects can be given to improve programming skills.

PRINCIPLES OF COMMUNICATION SYSTEMS		Semester	4
Course Code	BEC403	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3
Examination nature (SEE)	Theory/practical		
Course objectives: This course will enable students to • Understand and analyse concepts of Analog Modulation schemes viz; AM, FM • Design and analyse the electronic circuits for AM and FM modulation and demodulation. • Design and analyse the electronic circuits used at various stages of RF transmitter and receiver. • Understand and analyse concepts of digitization of signals. • Evolve the concept of SNR in the presence of channel induced noise			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. 1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. 2. Show Video/animation films to explain evolution of communication technologies. 3. Encourage collaborative (Group) Learning in the class. 4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. 6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
MODULE-1			
Amplitude Modulation Fundamentals: AM Concepts, Modulation index and Percentage of Modulation, Sidebands and the frequency domain, AM Power, Single Sideband Modulation. AM Circuits: Amplitude Modulators, Amplitude Demodulators, Balanced Modulators (Lattice type).			
MODULE-2			
Fundamentals of Frequency Modulation: Basic Principles of Frequency Modulation, Principles of Phase Modulation, Modulation index and sidebands, Noise Suppression effects of FM, Frequency Modulation versus Amplitude Modulation. FM Circuits: Frequency Modulators: , Frequency Demodulators			
MODULE-3			

Radio Transmitters: Transmitter Fundamentals: Transmitter Configurations, Carrier Generators: Crystal Oscillators, Frequency Synthesizers, Phase Locked Loop Synthesizers. Communication Receivers: Basic Principles of Signal reproduction, Superheterodyne Receivers, Frequency Conversion: Mixing principles, Mixer and Converter Circuits, Local Oscillators and Frequency Synthesizers, Intermediate Frequency and Images.
MODULE-4
Digital communication Techniques: Digital transmission of data, parallel and serial Transmission, Data Conversion: Basic Principles of Data Conversion, D/A Converters, A/D Converters, ADC Specifications, Pulse Modulation: Comparing Pulse Modulation Methods, Pulse-Code Modulation.
MODULE-5
Noise: Signal to Noise Ratio, External Noise, Internal Noise, Expressing Noise Levels, Noise in Cascade Stages. Multiplexing and Demultiplexing: Multiplexing Principles, Frequency Division Multiplexing, Time Division Multiplexing, Pulse code Modulation: PCM Multiplexers, Demultiplexers, Benefits, Digital Carrier Systems (T carrier System) , Duplexing.

PRACTICAL COMPONENT OF IPCC (*Experiments can be conducted using a suitable circuit simulation software or hardware components*)

Sl.N O	Experiments
1	Design and Test the Amplitude Modulation and demodulation using diode and transistors.
2	Design and Test the Frequency modulation using VCO and demodulation using slope detector circuit.
3	Design and test a high power a) Class A line RF amplifier. b) Class E RF amplifier
4	Design and test a mixer used for frequency translation.
5	Design and test a VCO used for local oscillator service
6	Verification of Sampling Theorem using sampling a sinusoidal signal using a sample and hold circuit.
7	TDM PAM Multiplexer and Demultiplexer
8	A String DAC and Flash Converter (Demo Experiment)
9	Design and Test a RF Transmitter circuit (Demo Experiment)
10	Design and Test a RF Receiver circuit (Demo Experiment)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the amplitude and frequency modulation techniques and perform time and frequency domain transformations.
2. Identify the schemes for amplitude and frequency modulation and demodulation of analog signals and compare the performance.
3. Characterize the influence of channel noise on analog modulated signals.
4. Define the schemes for sampling, pulse amplitude modulation and pulse code modulation systems.
5. Design of circuits used in different stages of communication transmitters and receivers.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be

conducted for 50 marks and scaled down to **10 marks**.

- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

9. The question paper will have ten questions. Each question is set for 20 marks.
10. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
11. The students have to answer 5 full questions, selecting one full question from each module.
12. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.

Reference Books

9. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1
10. B P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems", Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.

11. Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7.

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Communication Laboratory		Semester	4
Course Code	BECL404	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	3
Examination type (SEE)	Practical		
Course objectives: This laboratory course enables students to • Understand the basic concepts of AM and FM modulation and demodulation. • Design and analyse the electronic circuits used for AM and FM modulation and demodulation circuits. • Understand the sampling theory and design circuits which enable sampling and reconstruction of ofanalog signals. • Realize the electronic circuits to perform pulse amplitude modulation, pulse code modulation and s and multiplexing. • Understand the working principles of RF transmitters and receivers.			
	Experiments		
1	Design and plot the frequency response of an active band pass and band stop filters.		
2	Design and test a high-level collector Modulator circuit and Demodulation the signal using diode detector.		
3	Test the Balanced Modulator / Lattice Modulator (Diode ring)		
4	Frequency modulation using VCO and PLL FM demodulator.		
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii)Pulse amplitude modulation and demodulation.		
6	Design and test the Time Division Multiplexing of two bandlimited signals		
7	Design and test BJT/FET Mixer		
8	Design and test the Pulse width Modulation and Pulse Position Modulation.		
	Demonstration Experiments (For CIE)		
9	PLL Frequency Synthesizer		
10	PAM Multiplexer and Demultiplexer		
11	PCM Multiplexer and Demultiplexer		
12	Low power RF Transmitter and Receiver operations.		

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the basic concepts of RF transmitters and Receivers.
2. Illustrate the AM and FM modulation generation and detection using suitable electronic circuits.
3. Design and test the sampling, Multiplexing and pulse modulation techniques using electronic hardware.
4. Design and Demonstrate the electronic circuits used for RF transmitters and receivers.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.

8051 MICROCONTROLLER		Semester	4
Course Code	BEC405A	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: • Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers. • Familiarize the basic architecture of 8051 microcontroller. • Program 8051 microprocessor using Assembly Level Language and C. • Understand the interrupt system of 8051 and the use of interrupts. • Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051. Interface 8051 to external memory and I/O devices using its I/O ports.			
Teaching-Learning Process (General Instructions) The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: 1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes. 2. Show Video/animation films to explain the functioning of various techniques. 3. Encourage collaborative (Group) Learning in the class 4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. 6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding. Give Programming Assignments.			
Module-1			
8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing.			
Module-2			
8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions			
Module-3			

8051 Stack, I/O Port Interfacing and Programming: 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops - Delay subroutine, Factorial of an 8 bit number (result maximum 8 bit), Block move without overlap, Addition of N 8 bit numbers, Picking smallest/largest of N 8 bit numbers.

Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status.

Module-4

8051 Timers and Serial Port: 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin.

8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially

Module 5

8051 Interrupts and Interfacing Applications: 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. Interfacing 8051 to ADC-0804, LCD and Stepper motor and their 8051 Assembly language interfacing programming

Course outcome (Course Skill Set)

At the end of the course, students will be able to:

1. Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.
2. Write 8051 Assembly level programs using 8051 instruction set.
3. Explain the Interrupt system, operation of Timers/Counters and Serial port of 8051.
4. Write 8051 Assembly language program to generate timings and waveforms using 8051 timers, to send & receive serial data using 8051 serial port and to generate an external interrupt using a switch.
5. Write 8051 C programs to generate square wave on 8051 I/O port pin using interrupt and to send & receive serial data using 8051 serial port. Interface simple switches, simple LEDs, ADC 0804, LCD and Stepper Motor to 8051 using 8051 I/O ports.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- ☐ There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- ☐ Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- ☐ Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- ☐ The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:**Books**

1. The 8051 Microcontroller and Embedded Systems – using assembly and C ", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/ Cengage Learning

REFERENCE BOOKS:

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
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Industrial Electronics		Semester	4
Course Code	BEC405 B	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
Course objectives: This course will enable student to • Explain broad types of industrial power devices, there structure, and its characteristics. • Design and analyse the broad categories of power electronic circuits. • Explain various types of MEMs devices, principle of operation and construction. • Familiarize with soft core processors and computer architecture. • Apply protective methods for devices and circuits.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various courseoutcomes. 1. Lecture method (L) does not mean only traditional lecture method, but different type of teachingmethods may be adopted to develop the outcomes. 2. Show Video/animation films to explain evolution of communication technologies. 3. Encourage collaborative (Group) Learning in the class. 4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes criticalthinking. 5. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop thinking skillssuch as the ability to evaluate, generalize, and analyze information rather than simply recall it. 6. Show the different ways to solve the same problem and encourage the students to come up with theirown creative ways to solve them. 7. Discuss how every concept can be applied to the real world - and when that's possible, it helpsimprove the students' understanding.			
Module-1			
Industrial Power Devices: General purpose power diodes, fast recovery power diodes, schottky power diodes, silicon carbide power diodes (Text book 1: 2.5, 2.6), Power MOSFETs, Steady state characteristics, switching characteristics, silicon carbide MOSFETs, COOLMOS, Junction field effect transistors, operation and characteristics of JFETs, Silicon Carbide JFET structures, Bipolar Junction Transistors, Steady state characteristics, switching characteristics, silicon carbide BJTs, IGBT, silicon carbide IGBTs (Text book 1: 4.3, 4.4, 4.6, 4.7), Thyristor, Thyristor characteristics, two transistor model (Text book 1: 9.2, 9.3, 9.4).			
Module-2			

Power Electronics Circuits: Controlled Rectifiers – Single phase full converter with R and RL load, Single phase dual converters, and Three phase full converter with RL load (Text book 1: 10.2, 10.3, 10.4). Switching mode regulators – Buck Regulator, Boost regulator, Buck – Boost regulator, comparison of regulators (Text book 1: 5.9.1, 5.9.2, 5.9.3, 5.10) Inverters – Principle of operation, Single phase bridge inverter, Three phase inverter with 180 and 120 degree conduction, Current source inverter (Text book 1: 6.3, 6.4, 6.5, 6.9). AC voltage controllers – Single phase full wave controller with resistive load, single phase full wave controller with inductive load (Text book 1: 11.3, 11.4).
Module- 3
MEMS Devices: Sensing and Measuring Principles, Capacitive Sensing, Resistive Sensing, Piezoelectric Sensing, Thermal Transducers, Optical Sensors, Magnetic Sensors, MEMS Actuation Principles, Electrostatic Actuation, Thermal Actuation, Piezoelectric Actuation, Magnetic Actuation, MEMS Devices Inertial Sensors, Pressure Sensors, Radio Frequency MEMS: Capacitive Switches and Phase Shifters, Microfluidic Components, Optical Devices. (Text book 2: 13.1, 13.3, 13.4)
Module- 4

Soft Core Processors - Processor Core Options, Processor Definition Process, Software Development Aspects, Utilization of Soft-Core Processors, Custom Instructions, Soft-Core Processor on an ASIC vs. FPGA, Design Issues, Applications for Soft-Core Processors (**Text book 2: 22.2, 22.3, 22.4, 22.5, 22.6, 22.7, 22.8, 22.9**).

Computer Architecture - Hardware Organization, Computer Software, Programming Languages, Operating Systems, Information Representation in Digital Computers, Computer Programming Model, CPU Registers, Immediate Operands, Memory, Organization, Memory Addressing, Computer Instruction, Types, Interrupts and Exceptions, Evaluating Instruction Set Architectures, Computer System Design, Hierarchical Memory Systems, Memory Characteristics, Semiconductor Memory Technologies, Memory System Organization, Cache Memory, Virtual Memory Management, Interfaces to Input/Output Devices, Microcontroller Architectures

Multiple Processor Architectures (**Text book 2: 23.2, 23.3, 23.4, 23.5, 23.6, 23.7, 23.8, 23.9, 23.10**)

Module- 5

Protections of Devices and Circuits: Cooling and Heat sinks, Thermal Modeling of Power Switching Devices, Electrical Equivalent Thermal model, Mathematical Thermal Equivalent Circuit, Coupling of Electrical and Thermal Components, Snubber circuits, Reverse Recovery Transients, Supply and Load side transients, Voltage protection by Selenium Diodes and Metaloxide Varistors, Current protection, Fusing, Fault current with AC source, Fault current with DC source, Electromagnetic Interference, sources of EMI, Minimizing EMI Generation, EMI shielding, EMI standards (**Text book 1: 17.2, 17.3, 17.4, 17.5, 17.6, 17.7, 17.8, 17.9**).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain different types of industrial power devices such as MOSFET, BJT, IGBT etc, their structure, and its operating characteristics.
2. Design and analyse the power electronic circuits such as switch mode regulators, inverters, controlled rectifiers and ac voltage controllers.
3. Explain various types of MEMS devices used for sensing pressure, temperature, current, voltage, humidity, vibration etc..
4. Familiarize with soft core processors such as ASIC and FPGA.
5. Familiarize with computer hardware, software, architecture, instruction set, memory organization, multiprocessor architecture.
6. Apply protective methods for devices various industrial power devices based on thermal requirements and develop protective methods for the circuits against various electrical parameters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- ☐ There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- ☐ Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- ☐ Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- ☐ The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:**Books**

1. Power Electronics: Devices, Circuits, and Applications, Muhammad H. Rashid, Pearson, 4th International edition.
2. Fundamentals of Industrial Electronics, Bogdan M. Wilamowski, J. David Irwin, CRC Press, 2011,
3. Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall.
4. Ned Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics: Converters, Applications and Design", Wiley India Ltd, 2008.

Web links and Video Lectures (e-Resources):

- <https://archive.nptel.ac.in/courses/108/102/108102145/>
- <https://nptel.ac.in/courses/117105082>
- <https://www.youtube.com/channel/UCKg8GNii0Q-ieXE56AXosGg/featured>
- <https://www.ieee-ies.org/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz and Seminars

Operating system		Semester	4
Course Code	BEC405C	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand the different approaches of memory management and virtual memory management,
- Describe the structure and organisation of the file system.
- Understand inter process communication and dead lock situations.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method(L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Operating System: OS, goals of an OS, Computational structures, resource allocation techniques, efficiency, system performance and user convenience, classes operating system, batch processing, multiprogramming, time sharing system, real time and distributed operating systems.

(Topics from sections 1.2,1.3,2.2 to 2.8 of text 1).

Module-

2
Process Management: OS view of processes, PCB, Fundamental state, Transitions of a process, Threads, Kernel and User level Threads, Non-Preemptive Scheduling-FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling Linux . (Topics from sections 3.3,3.3.1,3.4,3.4.1,3.4.2, Selected scheduling topics from 4.2 and 4.3,4.6,4.7 of Text 1)
Module- 3

Memory Management: Contiguous Memory Allocation, Non-contiguous Memory Allocation, Paging, Segmentation with Paging, Virtual Memory Management, Demand Paging, VM Handler, FIFO, LRU Page replacement policies, Virtual memory in Unix and Linux. (Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except optimal policy and 6.3.1, 6.7, 6.8 of Text 1).
Module-4
File systems: File systems and IOCS, File Operation, File Organization, Directory Structure, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access. (Topics from section 7.1 to 7.8 of Text).
Module-5
Message passing and deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlocks detection algorithm, Deadlocks Prevention. (Topics from sections 10.1 to 10.3, 11.1 to 11.5 of Text).
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Explain the goals, structure, operation and types of operating system. 2. Apply scheduling techniques to find performance factors. 3. Explain organization of file system and IOCS. 4. Apply suitable techniques for contiguous and non contiguous memory allocation. 5. Describe message passing, deadlock detection and prevention methods.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- ☐ There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- ☐ Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- ☐ Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- ☐ The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:**Books**

1. Operating system – A concept based Approach, by Dhamdhare, TMH, 2nd edition.

Web links and Video Lectures (e-Resources):

- <https://archive.nptel.ac.in/courses/106/105/106105214/>
- https://onlinecourses.nptel.ac.in/noc20_cs04/preview
- https://onlinecourses.nptel.ac.in/noc21_cs72/preview
- <https://nptel.ac.in/courses/106106144>
- <https://nptel.ac.in/courses/106102132>
- <https://nptel.ac.in/courses/106106168>
- <https://archive.nptel.ac.in/courses/106/102/106102132/>.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Real world problem solving using group discussion.
- Role play for process scheduling.
- Present animation for deadlock.
- Real world example of memory management concepts.

Control Systems		Semester	4
Course Code	BEC405D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: • Understand the basic features, configurations and application of control systems. • Understand various terminologies and definitions for the control systems. • Learn how to find a mathematical model of electrical, mechanical and electro- mechanical systems. • Know how to find time response from the transfer function. • Find the transfer function via Mason's rule. • Analyze the stability of a system from the transfer function.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. • Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. • Encourage collaborative (Group) Learning in the class. • Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking. • Adopt Problem Based Learning (PBL), which fosters students Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in a multiple representation. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding. • Adopt Flipped class technique by sharing the materials/ Sample Videos prior to the class and have discussions on the topic in the succeeding classes.			
Module-1			
Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical Systems, Electrical Systems, Electro mechanical systems, Analogous Systems.			
Module-2			
Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs.			
Module-3			

Time Response of feedback control systems: Standard test signals, Unitstep response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design).
Module-4
Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion. Introduction to Root-Locus Techniques, The root locus concepts, Construction of root loci. Frequency domain analysis and stability: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function.
Module-5
Introduction to Polar Plots, (Inverse Polar Plots excluded) Mathematical preliminaries, Nyquist Stability criterion, (Systems with transportation lag excluded) Introduction to lead, lag and lead-lag compensating networks (excluding design). Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations.
Course outcome (Course Skill Set) At the end of the course, the student will be able to : - Develop the mathematical model of mechanical and electrical systems. - Develop transfer function for a given control system using block diagram reduction techniques and signal flow graph method. - Determine the time domain specifications for first and second order systems. - Determine the stability of a system in the time domain using Routh- Hurwitz criterion and Root-locus technique. - Determine the stability of a system in the frequency domain using Nyquist and bode plots.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

13. The question paper will have ten questions. Each question is set for 20 marks.

14. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions) ~~should have a mix of topics under that module~~

Suggested Learning Resources:**Book**

1. J. Nagarath and M. Gopal, "Control Systems Engineering", New Age International(P) Limited, Publishers, Fifth edition- 2005, ISBN:81- 224-2008-7.

ReferenceBooks:

1. "Modern Control Engineering", K.Ogata, Pearson Education Asia/PHI, 4th Edition, 2002. ISBN978-81 -203-4010- 7.
2. "Automatic Control Systems", Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th Edition, 2008.
3. "Feedback and Control System," Joseph J Distefano III et.al., Schaum's Outlines, TMH, 2nd Edition 2007.

Web links and Video Lectures (e-Resources):
• .
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

Embedded C Basics		Semester	4
Course Code	BEC456A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	2
Examination type (SEE)	Theory/practical/Viva-Voce /Term-work/Others		
Course objectives: This course will enable students to: • Understand the basic programming of Microprocessor and microcontroller. • Develop the microcontroller-based programs for various application in simulation environment • Program a microcontroller to control an external hardware using suitable I/O ports.			
Sl.N O	Experiments		
	Conduct the following experiments by writing C Program using Keil microvision simulator (any 8051 microcontroller can be chosen as the target).		
1	Write a 8051C program to multiply two 16 bit binary numbers.		
2	Write a 8051 C program to find the sum of first 10 integer numbers.		
3	Write a 8051 C program to find factorial of a given number.		
4	Write a 8051 C program to add an array of 16bit numbers and store the 32 bit result in internal RAM		
5	Write a 8051C program to find the square of a number (1to10)using look-up table.		
6	Write a 8051 C program to find the largest/smallest number in an array of 32 numbers		
7	Writea8051 C program to arrange a series of 32bit numbers in ascending/descending order		
8	Write a 8051 C program to count the number of ones and zeros in two consecutive memory locations		
9	Write a 8051C program to scan a series of 32bit numbers to find how many are negative.		
10	Writea8051 C program to display “HelloWorld” message (either in simulation mode or interface an LCD display).		
11	Write a 8051C program to generate the waveforms: square, triangle and ramp, using DAQ.		
12	Write a 8051 C program to run a stepper motor in clock wise and counter clockwise direction with a given step angle.		

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C programs in 8051 for solving simple problems that manipulate input data using different instructions.
2. Develop testing and experimental procedures on 8051 Microcontroller, analyze their operation under different cases.
3. Develop programs for 8051 Microcontroller to implement real world problems.
4. Develop microcontroller applications using external hardware interface.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners

jointly.

- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

“The8051Microcontroller:Hardware,SoftwareandApplications”,VUdayashankaraandMSMallikarjuna Swamy, McGrawHillEducation,1stedition,2017.

PCB Design		Semester	4
Course Code	BEC456B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy		Total Marks	100
Credits	01	Exam Hours	1
Examination type (SEE)	Theory		
Course objectives: • Study about layout planning, art work and design of PCB • To understand the PCB production process • Discuss the role of Modern trends and automatic design of PCB			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes 2. Show Video/animation films to explain the functioning of various 3. Encourage collaborative (Group) Learning in the class to promote critical thinking 4. Topics for seminars on several MEMS related topics and their applications 5. Encourage the students to take up mini projects and main projects 6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Design of Printed Circuit Boards:Layout Planning: Introduction, General Consideration, PCB Sizes, Layout Approaches, Documentation, Layout, General Rules and Parameters: Introduction, Resistance, Capacitance, Inductance of PCB conductors, Conductor Spacing, Component Placing and Mounting, Cooling Requirements and Package Density, Layout Check, Art work.			
Module-2			
Technology of PCB: Film Master Production: Introduction, Emulsion Parameters, Film Emulsions, Dimensional Stability of Film Masters, Reprographic Cameras, Darkroom, Film Processing, Film Registration, Properties of Copper Clad Laminates: Introduction, Manufacture of Copper Clad Laminates, Properties and Types of Laminates, Specifications and Test Methods, Board cleaning before Pattern Transfer: Manual and Machine Cleaning Processes.			
Module-3			
Photoprinting: Basic Processes for Double Sided PCBs, Photoresists, Wet Film Resists, Coating Processes, Exposure and further Processing of Wet Film Resists, Dry Film Resists. Screen Printing: Screen Fabrics, Screen and Frame Preparation, Pattern Transfer onto the screen, Reclamation of the Screen Fabrics, Printing, Trouble shooting			
Module-4			
Plating: Introduction, Immersion Plating, Electroless Plating, Electroplating, Plating Quality Control, Etching, Etching Machines, Etchant Systems, Minimising Pollution, Mechanical Machining operations. Multilayer Boards: Introduction, Design and Test Considerations,			

Multilayer Construction, Equipment, Laminating Process and further processing.

Module-5

PCB Technology Trends: Fine line conductors with Ultra-Thin Copper Foil, Multilayer and Multiwire Boards, Flexible Printed Circuit Boards. **Automation and Computers in PCB Design:** Automated Artwork Draughting, Computer Aided Design, Design Automation.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

11. Define the detailed circuit diagram and prerequisite before the actual PCB layout.
12. Understand the process of PCB production and Material selection
13. Understand the PCB fabrication by transferring the conductor pattern on base material
14. Know about the Plating techniques, Etching process and multilayer PCB board construction
15. Understand about new streams in PCB technology and modern facilities for PCB design

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Question Paper Type MCQ

Suggested Learning Resources:**Books**

2. Printed Circuit Boards-Design & Technology by Walter C Bosshart, Tata Mc Graw-Hill Pvt.Ltd, 2010
3. Printed Circuit Boards-Design, Fabrication, Assembly and Testing by Dr.R.S. Khandapur, Mc Graw-Hill Education, 2017

Web links and Video Lectures (e-Resources):

- PCB designing software YouTube links
- NPTEL courses and videos

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- PCB making for simple electronic circuit and testing
- Quizzes and seminar

DAQ using Lab VIEW		Semester	4
Course Code	BEC456C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	2
Examination type (SEE)	Theory/Practical/Viva-Voce /Term-work/Others		
Course objectives: This course will enable students to: • Process the knowledge of loop constructs. • Fundamentals of graphical programming and use Lab VIEW modules • Implement ‘Timing’ functions. • Input algebraic formulas via ‘Formula Nodes’ and ‘Expression Nodes’.			
Sl.N O	Experiments		
1	Data acquisition using LabVIEW for temperature measurement with thermocouple.		
2	Data acquisition using LabVIEW for temperature measurement with AD590.		
3	Data acquisition using LabVIEW for temperature measurement with RTD.		
4	Data acquisition using LabVIEW for temperature measurement with Thermistor.		
5	Creation of a CRO using LabVIEW and measurement of frequency and amplitude from external source.		
6	Create function generator using LabVIEW and display the amplitude and frequency on CRO (externally connected)		
7	Demonstrate amplitude modulation considering modulating and carrierwave from external source.		
8	Interface LEDs to DAQ output and implement counter.		
9	Data acquisition using LabVIEW for load/strain measurement using suitable transducers.		
10	Demonstrate binary to greyscale converter (&viceversa) using DAQ card.		
11	Data acquisition using LabVIEW for distance/humidity measurement using suitable transducers.		
12	Reading audio input with Microphones and output using DAQ card.		

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

5. Build temperature indicating instruments using LabVIEW(NIDAQ)
6. Interface peripheral devices/instruments to LabVIEW
7. Build LabVIEW modules to sense and process audio inputs
8. Apply programming structures, data types, and the analysis and signal processing algorithms in LabVIEW

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners

jointly.

- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI,2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGrawHill,SecondEdition,2011.

Risk Management in IoT Implementation		Semester	IV
Course Code	BEC456D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	14	Total Marks	100
Credits	01	Exam Hours	1
Examination type (SEE)	Theory/practical		
Course objectives:			
☐ Understand the fundamental concepts and principles of the Internet of Things (IoT) and its relevance in various industries. Identify and assess potential risks and challenges associated with implementing IoT projects.			
☐ Develop effective risk management strategies and mitigation plans specific to IoT implementations. Implement security controls and best practices to ensure the confidentiality, integrity, and availability of IoT systems.			
☐ Comply with relevant regulations and standards to address data privacy, security, and ethical considerations in IoT implementations.			

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

- Active Learning: Encourage students to actively engage in the learning process through hands-on activities, group discussions, case studies, and problem-solving exercises.
- Real-World Examples and Case Studies: Provide real-world examples and case studies related to IoT implementations and risk management.
- Collaborative Learning: Foster collaborative learning environments where students can work together in groups or teams to analyse and solve IoT-related challenges.
- Simulations and Hands-on Experiments: Incorporate simulations or hands-on experiments that replicate IoT scenarios and risk management challenges.
- Formative Assessments and Feedback: Implement regular formative assessments throughout the course to gauge students' progress and understanding of the course outcomes.

Module-1**Introduction to IoT and Risk Management**

Overview of the Internet of Things (IoT) and its applications; Understanding the importance of risk management in IoT implementation; Key components of risk management in IoT; Common risks and challenges in IoT implementation; Case studies and examples of successful and failed IoT implementations.

Module-2**Identifying and Assessing Risks in IoT**

Identification of potential risks in IoT implementation; Risk assessment methodologies and techniques for IoT projects; Threat modelling and risk analysis in IoT systems; Assessing the impact and likelihood of identified risks; Prioritization of risks based on their significance.

Module-3

Mitigation Strategies for IoT Risks Developing a risk mitigation plan for IoT projects; Security controls and best practices for IoT devices and networks; Data privacy and protection measures in IoT systems; Implementing secure communication protocols in IoT; Securing IoT gateways and cloud platforms.
Module-4
Monitoring and Response to IoT Risks Real-time monitoring of IoT devices and networks; Intrusion detection and prevention in IoT systems; Incident response planning for IoT security breaches; Continuous monitoring and vulnerability management in IoT; Data backup and disaster recovery strategies for IoT systems.
Module-5
Compliance and Regulatory Considerations Overview of relevant regulations and standards for IoT implementation; Compliance requirements for data privacy and security in IoT; Impact of industry-specific regulations on IoT projects; Role of audits and assessments in ensuring compliance; Ethical considerations and responsible use of IoT technologies.
Course outcome (Course Skill Set) At the end of the course the student will be able to: • Students will be able to explain the core concepts and applications of the Internet of Things and its impact on industries and society. Students will be able to identify and assess risks and challenges in IoT implementations, applying appropriate methodologies and techniques. • Students will be able to develop comprehensive risk management strategies and mitigation plans tailored to specific IoT projects. Students will be able to implement security controls and best practices to protect IoT devices, networks, and data from potential threats and vulnerabilities. • Students will be able to analyse and comply with relevant regulations, standards, and ethical considerations to ensure responsible and secure IoT implementations.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour**. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

OR

MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then

1. The question paper will have ten questions. Each question is set for 10 marks.
2. There will be 2 questions from each module. Each of the two questions under a module may or may not have the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

1. MindMatrix.io
2. "Practical IoT Security: A Guide to Building Secure Connected Systems" by Brian Russell, Drew Van Duren, and John R. Scharlau
3. "Internet of Things: Principles and Paradigms" by Rajkumar Buyya, Amir Vahid Dastjerdi, and Sriram Venugopal
4. "IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things" by David Hanes, Gonzalo Salgueiro, and Patrick Grossetete

5. "Managing Risk and Security in the Internet of Things: Frameworks and Best Practices" by TimLister, Brian Russell, and Tom Olzak
6. "The Internet of Risky Things: Trusting the Devices That Surround Us" by Sean Smith and AbelSanchez

Web links and Video Lectures (e-Resources):

- makes.mindmatrix.io

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Risk Assessment and Mitigation Plan Development: Divide students into small groups and assign them different IoT implementation scenarios.
- Threat Modelling Exercise: Provide students with a sample IoT system architecture. In pairs or individually, students should conduct a threat modelling exercise, identifying potential threats and vulnerabilities in the system.
- IoT Security Audit and Compliance Assessment: Ask students to conduct a security audit and compliance assessment of a hypothetical IoT deployment. Provide them with a checklist of relevant security controls, regulatory requirements, and industry standards.
- IoT Risk Simulation Game: Develop a simulation game where students take on different roles in an IoT implementation team, such as project manager, security analyst, or compliance officer.
- Case Studies and Problem-Solving Exercises: Assign real-world case studies or problem-solving exercises related to IoT risk management. Students should analyse the given scenarios, identify risks, propose mitigation strategies, and present their solutions.

V Semester

Technological Innovation Management & Entrepreneurship			Semester	V
Course and Course Code	HSMS	BXX501	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0		SEE Marks	50
Total Hours of Pedagogy	40 hours		Total Marks	100
Credits	3		Exam Hours	3
Examination nature (SEE)	Theory			
Course objectives: After completion of the course, the students will be able to • Understand basic skills of Management • Understand the need for Entrepreneurs and their skills • Identify the Management functions and Social responsibilities. • Understand the identification of Business, drafting the Business plan and sources of funding.				
Teaching-Learning Process (General Instructions) These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes. • Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes. • Show Video/animation films to explain the functioning of various techniques. • Encourage collaborative (Group) Learning in the class • Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking • Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. • Topics will be introduced in multiple representations. • Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. • Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.				
MODULE – 1				
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession (Selected topics of Chapter 1, Text 1). Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making(Text 1).				
Teaching-Learning Process		Chalk and talk method, YouTube Videos, Power Point Presentation.		
RBT Levels		L2, L3		
MODULE – 2				
Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization-Process Departmentalization, Purpose Departmentalization ,Committees- Meaning, Types of Committees. Staffing-Need and Importance, Recruitment and Selection Process.				

Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation- Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication (Text 1).	
Teaching-Learning Process RBT Levels	Chalk and talk method, YouTube Videos, Power Point Presentation. L2, L3
MODULE – 3	
Leadership -Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (Text 1). Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance (Text 1).	
Teaching-Learning Process RBT Levels	Chalk and talk method, YouTube Videos, Power Point Presentation. L1, L2, L3
MODULE – 4	
Entrepreneurship: Introduction, Evolution of the concept of Entrepreneurship, Entrepreneurship today, Types of Entrepreneurs, Entrepreneurship, Entrepreneurial competencies, Capacity Building for Entrepreneurs. Identification of Business Opportunities: Introduction, Mobility of Entrepreneurs, Business opportunities in India, Models for opportunity Evaluation.	
Teaching-Learning Process RBT Levels	Chalk and talk method, YouTube Videos, Power Point Presentation. L1, L2, L3
MODULE – 5	
Business plans: Introduction, purpose of a Business plan, contents of a Business plan, presenting a Business plan, why do some Business plan fail? Procedure for setting up an Enterprise. Institutions supporting Business opportunities: Central level institutions- National Board for micro, small & medium Enterprises(NBMSME), MSME-DO, National Small Industries Corporation. State level institutions- state Directorate Industries and commerce, District Industries Centres, state financial Corporations, State Industrial Development Corporation(SIDC), State Industrial Area Development Board (SIADB). Other Institutions - NABARD, Technical consultancy organisation (TCO), Small Industries Development Bank of India(SIDBI), Export Promotion Councils, Non governmental Organisations.	
Teaching-Learning Process RBT Levels	Chalk and talk method, YouTube Videos, Power Point Presentation. L1, L2, L3
Course outcomes (Course Skill Set): At the end of the course, the student will be able to: 1) Understand the fundamental concepts of Management and its functions. 2) Understand the different functions to be performed by managers/Entrepreneur. 3) Understand the social responsibilities of a Business. 4) Understand the Concepts of Entrepreneurship and to identify Business opportunities. 5) Understand the components in developing a business plan and awareness about various sources of funding and Institutions supporting Entrepreneur.	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/	

course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

- 1) Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
- 2) Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, 2nd Edition, Pearson Education 2018, ISBN 978-81-317-6226-4.

Reference Books

- 1) Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/courses/110107094>
- <https://nptel.ac.in/courses/110106141>
- <https://nptel.ac.in/courses/122106031>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes,
- Assignments,
- Seminars

OBJECT ORIENTED PROGRAMMING USING JAVA		Semester	V
Course Code	BUE502	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination Type (SEE)	Theory		
Course Objectives: - To learn primitive constructs in JAVA programming language. - To understand Object Oriented Programming Features of JAVA. - To gain knowledge on packages, multithreaded programming and exceptions.			
Teaching-Learning Process (General Instructions) These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes. - Use Online Java Compiler IDE: https://www.jdoodle.com/online-java-compiler/ or any other. - Demonstration of programming examples. - Chalk and board, Power point presentations. - Online material (Tutorials) and video lectures.			
MODULE-1			
Data Types, Variables, and Arrays: The Primitive Types (Integers, Floating-Point Types, Characters, Booleans), Variables, Type Conversion and Casting, Arrays. Operators: Arithmetic Operators, Relational Operators, Boolean Logical Operators, The Assignment Operator, The ? Operator, Operator Precedence. Control Statements: Java’s Selection Statements (if, The Traditional switch), Iteration Statements (while, do-while, for, Nested Loops), Jump Statements (Using break, Using continue, return). RBT Levels: L1, L2			
MODULE-2			
Introducing Classes: Class Fundamentals, Declaring Objects, Assigning Object Reference Variables, Introducing Methods, Constructors, The this Keyword. Methods and Classes: Overloading Methods, Objects as Parameters, Argument Passing, Returning Objects. RBT Levels: L1, L2			
MODULE-3			
Inheritance: Inheritance Basics, Using super, Creating a Multilevel Hierarchy, When Constructors Are Executed, Method Overriding, Using Abstract Classes. Interfaces: Interfaces, Default Interface Methods, Use static Methods in an Interface, Private Interface Methods. RBT Levels: L1, L2, L3			
MODULE-4			
Packages: Packages, Packages and Member Access, Importing Packages. Exceptions: Exception-Handling Fundamentals, Exception Types, Uncaught Exceptions, Using try and catch, Nested try Statements, throw, throws, finally, Java’s Built-in Exceptions. RBT Levels: L1, L2, L3			
MODULE-5			
Multithreaded Programming: The Java Thread Model, The Main Thread, Creating a Thread, Creating Multiple Threads, Using isAlive() and join(). Enumerations, Type Wrappers and Autoboxing: Enumerations (The values() and valueOf() Methods), Type Wrappers (Character, Boolean, The Numeric Type Wrappers), Autoboxing (Autoboxing and Methods). RBT Levels: L1, L2, L3			

PRACTICAL COMPONENT OF IPCC

Sl. No.	Experiments
1.	Write a JAVA program that prints all real solutions to the quadratic equation $ax^2+bx+c=0$. Read in a, b, c and use the quadratic formula.
2.	Create a JAVA class called Student with the following details as variables within it. • USN • Name • Branch • Phone Write a JAVA program to create n Student objects and print the USN, Name, Branch, and Phone of these objects with suitable headings.
3.	Write a JAVA program for Arithmetic calculator using switch case menu.
4.	Develop a JAVA program to add TWO matrices of suitable order N (The value of N should be read from command line arguments).
5.	Develop a JAVA program to create a class named shape. Create three sub classes namely: circle, triangle and square, each class has two member functions named draw () and erase (). Demonstrate polymorphism concepts by developing suitable methods, defining member data and main program.
6.	Write a JAVA program demonstrating Method overloading and Constructor overloading.
7.	Develop a JAVA program to raise a custom exception (user defined exception) for DivisionByZero using try, catch, throw and finally.
8.	Demo Experiment: Design a super class called Staff with details as Staff_ID, Name, Phone, Salary. Extend this class by writing three subclasses namely Teaching (domain, publications), Technical (skills), and Contract (period). Write a JAVA program to read and display at least 3 staff objects of all three categories.
9.	Demo Experiment: Develop a JAVA application to implement currency converter (Dollar to INR, EURO to INR, Yen to INR and vice versa), distance converter (meter to KM, miles to KM and vice versa), time converter (hours to minutes, seconds and vice versa) using packages.
Course Outcomes (Course Skill Set): At the end of the course, the student will be able to: CO 1: Demonstrate proficiency in writing simple programs involving branching and looping structures. CO 2: Design a class involving data members and methods for the given scenario. CO 3: Apply the concepts of inheritance and interfaces in solving real world problems. CO 4: Use the concept of packages and exception handling in solving complex problem. CO 5: Apply concepts of multithreading, autoboxing and enumerations in program development.	
Assessment Details (both CIE and SEE): The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are 25 marks and that for the practical component is 25 marks. CIE for the theory component of the IPCC: • 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus. • Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).	

- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC:

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks-25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Textbook:

1. Java: The Complete Reference, Twelfth Edition, by Herbert Schildt, November 2021, McGraw-Hill, ISBN: 9781260463422.

Reference Books:

1. Programming with Java, 6th Edition, by E Balagurusamy, Mar-2019, McGraw Hill Education, ISBN: 9789353162337.
2. Thinking in Java, Fourth Edition, by Bruce Eckel, Prentice Hall, 2006 (https://sd.blackball.lv/library/thinking_in_java_4th_edition.pdf)

Web links and Video Lectures (e-Resources):

- Java Tutorial: <https://www.geeksforgeeks.org/java/>
- Introduction To Programming In Java: <https://ocw.mit.edu/courses/6-092-introduction-to-programming-in-java-january-iap-2010/>
- Java Tutorial: <https://www.w3schools.com/java/>
- Java Tutorial: <https://www.javatpoint.com/java-tutorial>
- Installation of Java: https://www.java.com/en/download/help/index_installing.html
- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning:

- Demonstration of online IDEs like geeks for geeks, jdoodle or any other Tools.
- Demonstration of class diagrams for the class abstraction, type visibility, composition and inheritance.
- Programming Assignment / Course Project.

DIGITAL SYSTEM DESIGN USING VERILOG		Semester	V
Course Code	BUE503	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: 1. To know the basic language features of Verilog HDL and the role of HDL in digital logic design. 2. To know the behavioural modeling of combinational and simple sequential circuits. 3. To know the behavioural modeling of algorithmic state machines. 4. To know the synthesis of combinational and sequential descriptions. 5. To know the architectural features of programmable logic devices.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Chalk and Talk 2. PowerPoint Presentation and Videos 3. Flipped Classes 4. Practice session			
Module-1			
Introduction to Digital Design Methodology: Design Methodology-An Introduction, IC Technology Options. Review of Combinational Logic Design: Glitches and Hazards Introduction to Logic Design with Verilog : Structural models of combination logic, logic system, design verification and Test methodology, propagation delay, truth table models of combinational and sequential logic with verilog modules. RBT Level: L1,L2			
Module-2			
Logic Design With Behavioral Models of Combinational And Sequential Logic :Behavioral modeling, A Brief Look at data types for behavioural modeling, Boolean Equation-Based behavioral models of combinational logic, propagation delay and continuous assignments, latches and level sensitive circuits in verilog, cyclic behavioural models of flip flops and latches, cyclic behavior and edge detection, a comparison of styles for behavioral modelling. Behavioral Models of Multiplexers, Encoders, and Decoders, Dataflow Models of a Linear-Feedback Shift Register, Design Documentation with Functions and Tasks: Legacy or Lunacy? RBT Level: L1,L2,L3			
Module-3			
Logic Design With Behavioral Models of Combinational And Sequential Logic :Algorithmic State Machine Charts for Behavioral Modeling, Behavioral Models of Counters, Shift Registers, and Register Files Synthesis of Combinational and Sequential Logic : Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches RBT Level: L1,L2,L3			

Module-4	
Fundamentals of Sequential Logic Design: Design of Sequential Machines, State-Transition Graphs, Design Example: BCD to Excess-3 Code Converter, Serial-Line Code Converter for Data Transmission. Synthesis of Combinational and Sequential Logic: Synthesis of Explicit State Machines, Synthesis of Implicit State Machines, Registers and Counters. RBT Level: L1,L2,L3	
Module-5	
Programmable Logic and Storage Devices : Programmable Logic Devices, Storage Devices, Programmable Logic Array (PLA), Programmable Array Logic (PAL) ,Programmability of PLDs ,Complex PLDs (CPLDs) ,Field-Programmable Gate Arrays RBT Level: L1,L2	
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Demonstrate knowledge on HDL design flow, digital circuits design. 2. Design and develop the combinational and sequential circuits using behavioural modelling. 3. Solving algorithmic state machines using hardware description language. 4. Analyse the process of synthesizing the combinational and sequential descriptions. 5. Memorizing the advantages of programmable logic devices and their description in Verilog.	

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

TEXTBOOKS

1. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009

REFERENCE BOOK(s):

1. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.
2. Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Online Resources and Tutorials
- Verilog Simulation Projects
- Quiz
- Seminars

VERILOG LAB		Semester	V
Course Code	BUEL504	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
Total Hours of Pedagogy	12-14 slots	Exam Hours	2 Hours
Examination type (SEE)	Practical		
Course objectives: This course will enable students to: - Familiarize with the CAD tool to write HDL programs. - Understand simulation and synthesis of digital design. - Program FPGAs/CPLDs to synthesize the digital designs. - Interface hardware to programmable ICs through I/O ports.			
SL.NO	Write the Verilog Code, Simulate, Synthesize and Implement on the Hardware.		
1	Half Adder, Full Adder using three modelling styles		
2	Flip Flops: MS, RS, JK, D, T		
3	N-Bit Comparator		
4	a) 3:8 Decoder b) 8:3 Priority Encoder		
5	a) 4:1 Multiplexer b) 1:4 Demultiplexer c) BCD to Excess 3 Converter and vice versa d) Binary to Gray Converter and vice versa		
6	a) N-bit Synchronous Up-Down Counter b) N-bit Asynchronous Up-Down Counter		
7	a) 4-Bit Serial Shift Register b) 4 Bit Universal Shift Register		
	Interfacing Experiments		
8	Seven-Segment Light-Emitting Diode (LED) Display.		
9	Stepper motor		
10	ADC/DAC		
11	Elevator		
	Demonstration Experiments		
1.	UART protocol		
2.	I2C protocol		
Course outcomes (Course Skill Set): At the end of the course the student will be able to: - C01. Understanding of Hardware Description and Synthesis - C02. Problem-Solving and Analytical Thinking - C03. Synthesis and Optimization Skills - C04. Logical and Sequential Circuit Design - C05. Verilog Programming Proficiency			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- <https://nptel.ac.in/>

Digital Communication		Semester	V
Course Code	BUE515A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: - Understand the mathematical representation of signal, symbol, noise and channels. - Apply the concept of signal conversion to symbols and signal processing to symbols in transmitter and receiver functional blocks. - Compute performance issues and parameters for symbol processing and recovery in ideal and corrupted channel conditions.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Chalk and Talk. - Power Presentation and Videos. - Flipped Classes. - Practice Sessions.			
Module-1 Band-pass Signal to Equivalent Lowpass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low-pass representation of band pass systems, Complex representation of band pass signals and systems. Line codes: Uni-polar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities. RBT Levels: L1, L2			
Module-2 Signaling over AWGN Channels: Introduction, Geometric representation of signals, Gram Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel in to a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver. RBT Levels: L1, L2, L3			
Module-3 Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M-ary PSK,M-ary QAM. Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability. Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagram of Transmitter and Receiver. RBT Levels: L1, L2, L3			
Module-4 Digital Communication through Band Limited Channels: Characterization of Band-Limited Channels Signal Design for Band-Limited Channels, Design of Band-Limited Signals for No Inter symbol Interference—The Nyquist Criterion, Design of Band-Limited Signals with Controlled ISI—Partial-Response Signals, Data Detection for Controlled ISI, Signal Design for Channels with Distortion, Optimum Maximum-Likelihood Receiver, A Discrete-Time Model for a Channel with ISI. RBT Levels: L1, L2, L3			
Module-5 Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95. RBT Levels: L1, L2, L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

CO 1: Associate and apply the concepts of Band-pass sampling to well specified signals and channels.

CO 2: Analyze and compute performance parameters and transfer rates for low pass and band pass symbol under ideal and corrupted non-band limited channels.

CO 3: Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted band-limited channels.

CO 4: Demonstrate by simulation and emulation that band pass signals subjected to corrupted and distorted symbols in a band limited channel, can be demodulated and estimated at receiver to meet specified performance criteria.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Simon Haykin – Digital Communication Systems, John Wiley & sons, First Edition, 2014, ISBN978-0-471-64735-5.
2. John G Proakis and Masoud Salehi - Fundamentals of Communication Systems, 2014 Edition, Pearson Education, ISBN978-8-131-70573-5.

Reference Books:

1. B. P. Lathi and Zhi Ding - Modern Digital and Analog Communication Systems, Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.

2. Ian A Glover and Peter M Grant —Digital Communications, Pearson Education,Third Edition, 2010, ISBN 978-0-273-71830-7.
3. John G Proakis and Masoud Salehi — Communication Systems Engineering, 2nd Edition, Pearson Education, ISBN 978-93-325-5513-6.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz
- Seminar

ADVANCED COMPUTER ARCHITECTURE		Semester	V
Course Code	BUE515B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
Course objectives: • To make students understand the basic structure and operation of computer system • To measure the performance of architectures in terms of right parameters. • To understand the concepts of various memories. • To summarize parallel architecture and the software used for them.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.			
Module-1			
Theory of Parallelism: Parallel Computer Models, The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMD Computers, PRAM and VLSI Models, Program and Network Properties, Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws. For all Algorithm or mechanism any one example is sufficient.			
RBT Levels: L1, L2			
Module-2			
Hardware Technologies 1: Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology. For all Algorithms or mechanisms any one example is sufficient.			
RBT Levels: L1, L2			
Module-3			
Hardware Technologies 2: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential and Weak Consistency Models, Pipelining and Superscalar Techniques, Linear Pipeline Processors, Nonlinear Pipeline Processors. For all Algorithms or mechanisms any one example is sufficient.			
RBT Levels: L1, L2			
Module-4			
Parallel and Scalable Architectures: Multiprocessors and Multicomputers, Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Message-Passing Mechanisms, Multivector and SIMD Computers, Vector Processing Principles, Multivector Multiprocessors, Compound Vector Processing, Scalable, Multithreaded, and Dataflow Architectures, Latency-Hiding Techniques, Principles of Multithreading, Fine- Grain Multicomputer. For all Algorithms or mechanisms any one example is sufficient.			
RBT Levels: L3, L4			

Module-5	
Software for parallel programming: Parallel Models, Languages, and Compilers, Parallel Programming Models, Parallel Languages and Compilers, Dependence Analysis of Data Arrays. Instruction and System Level Parallelism, Instruction Level Parallelism, Computer Architecture, Contents, Basic Design Issues, Problem Definition, Model of a Typical Processor, Compiler-detected Instruction Level Parallelism ,Operand Forwarding ,Reorder Buffer, Register Renaming, Tomasulo's Algorithm. For all Algorithms or mechanisms any one example is sufficient.	
RBT Levels: L3, L4	
Course outcome (Course Skill Set) At the end of the course, the student will be able to : CO 1: Explain the concepts of parallel computing CO 2: Explain and identify the hardware technologies CO 3: Compare and contrast the parallel architectures CO 4: Illustrate parallel programming concepts	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
Continuous Internal Evaluation: - For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks. - The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered - Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. - For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.	
Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.	
Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). - The question paper will have ten questions. Each question is set for 20 marks. - There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. - The students have to answer 5 full questions, selecting one full question from each module. - Marks scored shall be proportionally reduced to 50 marks	
Suggested Learning Resources: Books Textbooks: John L.Hennessy and David A Patterson ,Computer architecture : A Quantitative approach ,Morgan	

Kaufmann ,6th edition ,2017. 2. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture (SIE): Parallelism, Scalability, Programmability, McGraw Hill Education 3/e. 2015 . Reference Books: 1. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Ninth Edition, 2012
Web links and Video Lectures (e-Resources):
WEB LINKS FOR REFERENCE • https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quiz • Seminar

Software Engineering and Project Management		Semester	V
Course Code	BUE515C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: - Outline software engineering principles and activities involved in building large software programs. - Identify ethical and professional issues and explain why they are of concern to Software Engineers. - Describe the process of requirement gathering, requirement classification, requirement specification and requirements validation. - Infer the fundamentals of object oriented concepts, differentiate system models, use UML diagrams and apply design patterns. - Explain the role of DevOps in Agile Implementation. - Discuss various types of software testing practices and software evolution processes. - Recognize the importance Project Management with its methods and methodologies. - Identify software quality parameters and quantify software using measurements and metrics.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. - Use of Video/Animation to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. - Introduce Topics in manifold representations. - Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. - Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1 Introduction: The evolving role of software, Software, The changing nature of software, Software engineering, A Process Framework, Process Patterns, Process Assessment, Personal and Team Process Models, Process Technology, Product and Process. Process Models: Prescriptive models, Waterfall model, Incremental process models, Evolutionary process models, Specialized process models. Requirements Engineering: Requirements Engineering Task, Initiating the Requirements Engineering process, Eliciting Requirements, Developing use cases, Building the analysis model, Negotiating Requirements, Validating Requirements, Software Requirement Document. RBT Levels: L1,L2			
Module-2			

Introduction, Modelling Concepts and Class Modelling: What is Object orientation? What is OO development? OO Themes; Evidence for usefulness of OO development; OO modelling history. Modelling as Design technique: Modelling, abstraction, The Three models. Class Modelling: Object and Class Concept, Link and associations concepts, Generalization and Inheritance, A sample class model, Navigation of class models, Introduction to RUP and UML diagrams. Building the Analysis Models: Requirement Analysis, Analysis Model Approaches, Data modelling. Concepts, Object Oriented Analysis, Scenario-Based Modeling, Flow-Oriented Modeling, class Based Modeling, Creating a Behavioral Model. RBT Levels: L2,L3
Module-3
Software Testing: A Strategic Approach to Software Testing, Strategic Issues, Test Strategies for Conventional Software, Test Strategies for Object -Oriented Software, Validation Testing, System Testing, The Art of Debugging. Agile Methodology & DevOps: Before Agile – Waterfall, Agile Development. Self-Learning Section: What is DevOps?, DevOps Importance and Benefits, DevOps Principles and Practices, 7 C's of DevOps Lifecycle for Business Agility, DevOps and Continuous Testing, How to Choose Right DevOps Tools?, Challenges with DevOps Implementation. RBT Levels: L3,L4
Module-4
Introduction to Project Management: Introduction, Project and Importance of Project Management, Contract Management, Activities Covered by Software Project Management, Plans, Methods and Methodologies, Some ways of categorizing Software Projects, Stakeholders, Setting Objectives, Business Case, Project Success and Failure, Management and Management Control, Project Management life cycle, Traditional versus Modern Project Management Practices. RBT Levels: L1,L2
Module-5
Activity Planning: Objectives of Activity Planning, When to Plan, Project Schedules, Sequencing and Scheduling Activities, Network Planning Models, Forward Pass– Backward Pass, Identifying critical path, Activity Float, Shortening Project Duration, Activity on Arrow Networks. Software Quality: Introduction, The place of software quality in project planning, Importance of software quality, software quality models, ISO 9126, quality management systems, process capability models, techniques to enhance software quality, quality plans. RBT Levels: L2,L3
Course outcome (Course Skill Set) At the end of the course, the student will be able to : CO 1: Understand the activities involved in software engineering and analyze the role of various process models. CO 2: Explain the basics of object-oriented concepts and build a suitable class model using modelling techniques. CO 3: Describe various software testing methods and to understand the importance of agile methodology and DevOps. CO 4: Illustrate the role of project planning and quality management in software development. CO 5: Understand the importance of activity planning and different planning models.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: - There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. - Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.
- Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

- Roger S. Pressman: Software Engineering-A Practitioners approach, 7th Edition, Tata McGraw Hill.
- Michael Blaha, James Rumbaugh: Object Oriented Modelling and Design with UML, 2nd Edition, Pearson Education, 2005.
- Bob Hughes, Mike Cotterell, Rajib Mall: Software Project Management, 6th Edition, McGraw Hill Education, 2018.
- Deepak Gaikwad, Viral Thakkar, DevOps Tools From Practitioner's Viewpoint, Wiley.
- Ian Sommerville: Software Engineering, 9th Edition, Pearson Education, 2012.

Reference Book:

- Pankaj Jalote: An Integrated Approach to Software Engineering, Wiley India.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Case study
- Field visit

ADVANCED IOT		Semester	V
Course Code	BUE515D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: - To understand the concepts of IOT and its applications in today's scenario. - To study the IoT network architecture and design. - To Understand IOT content generation and transport through networks use cases of IoT. - To Understand the devices employed for IOT data acquisition.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. - Use of Video/Animation to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. - Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. - Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
What is IoT?: Genesis of IoT, IoT and Digitization, IoT Impact – Connected Roadways, Connected Factory, Smart Connected Buildings, Smart Creatures, Convergence of IT and OT, Challenges. IoT Network Architecture and Design: Drivers behind new network Architectures, Simplified IoT Architecture. RBT Levels: L1,L2			
Module-2			
IoT Network Architecture and Design: Core IoT Functional Stack, Things Layer, Communication Network Layer – Access Network Sublayer, Gateways and Backhaul Sublayer, Network Transport Sublayer, IoT Network Management Sublayer. Applications and Analytics Layer, IoT Data Management and Compute Stack. RBT Levels: L2,L3			
Module-3			
Engineering IoT Networks-1: Things in IoT – Sensors, Actuators, MEMS and Smart Objects. WSN, Communications Criteria - Range, Frequency Bands, Power Consumption, Topology, Constrained Devices. Standard Alliances (LTE Cat0, Cat-M). RBT Levels: L2,L3			
Module-4			
Engineering IoT Networks-2: IP as IoT Network Layer – Key advantages of IP. Application Protocols for IoT – Transport Layer, IoT Application Layer Protocols (CoAP, MQTT). Data and Analytics for IoT – Structured and Unstructured data, Data in motion versus data at rest, IoT Data Analytics Overview and Challenges. RBT Levels: L2,L3			
Module-5			
IoT Use Cases: IoT in Industry - IoT Strategy for Connected manufacturing, Architecture for Connected Factory. Smart and Connected cities – Smart city network Architecture, Street layer, city layer, Data center layer, services layer. Smart street lighting. RBT Levels: L3,L4			

Course Outcome (Course Skill Set)

At the end of the course, the student will be able to :

CO 1: Understand the basic concepts IoT Architecture and devices employed.

CO 2: Analyze the sensor data generated and map it to IoT protocol stack for transport.

CO 3: Apply communications knowledge to facilitate transport of IoT data over various available communications media.

CO 4: Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.

CO 5: Apply knowledge of Information technology to design the IoT applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, "Cisco, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT", Pearson Education; First edition 2017, ISBN: 978-9386873743.
2. Arshdeep Bahga and Vijay Madisetti, "Internet of Things – A Hands on Approach", Orient Blackswan Private Limited - New Delhi; First edition.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz
- Seminar

COMPUTER NETWORKS		Semester	VI
Course Code	BUE601	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	30 hours Theory + 20 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		
Course objectives: • Fundamentals of data communication networks. • Software and hardware interfaces • Application of various physical components and protocols • Communication challenges and remedies in the networks.			
Teaching-Learning Process (General Instructions) These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) need not to be only traditional lecture method , but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. 6. Introduce Topics in manifold representations. 7. Shows the different ways to solve the same problem and encourage the students come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world- and when that's possible, it helps improve the students' understanding.			
MODULE-1			
Introduction to networks: Network hardware, Network software, Reference models, Physical Layer: Guided transmission media, Wireless transmission RBT Levels: L1,L2			
MODULE-2			
The Data link layer: Design issues of DLL, Error detection and correction, Elementary data link protocols, Sliding window protocols. RBT Levels : L2,L3			
MODULE-3			
The medium access control sub layer: The channel allocation problem, Multiple access protocols. Network Layer Design Issues, Routing Algorithms, Congestion Control Algorithms, QoS. RBT Levels : L2,L3			
MODULE-4			
The Transport Layer: The Transport Service, Elements of transport protocols, Congestion control, The internet transport protocols. RBT Levels : L2,L3			
MODULE-5			
Application Layer: Principles of Network Applications, The Web and HTTP, Electronic Mail in the Internet, DNS - The Internet’s Directory Service. RBT Levels : L3,L4			

PRACTICAL COMPONENT OF IPCC

Sl. NO.	Experiments
1	Implement Three nodes point-to-point network with duplex links between them for different topologies. Set the queue size, vary the bandwidth, and find the number of packets dropped for various iterations.
2	Implement simple ESS and with transmitting nodes in wire-less LAN by simulation and determine the throughput with respect to transmission of packets.
3	Write a program for error detecting code using CRC-CCITT (16-bits).
4	Implement transmission of ping messages/trace route over a network topology consisting of 6 nodes and find the number of packets dropped due to congestion in the network.
5	Write a program to find the shortest path between vertices using bellman-ford algorithm.
6	Implement an Ethernet LAN using n nodes and set multiple traffic nodes and plot congestion window for different source / destination.
7	Write a program for congestion control using leaky bucket algorithm.
Course outcomes (Course Skill Set): At the end of the course, the student will be able to: CO1 Learn the basic needs of communication system. CO2 Interpret the communication challenges and its solution. CO3 Identify and organize the communication system network components CO4 Design communication networks for user requirements.	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are 25 marks and that for the practical component is 25 marks . CIE for the theory component of the IPCC 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus. - Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks). - The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC. CIE for the practical component of the IPCC 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions. - On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day. - The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks. - The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.	

- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Textbooks:

1. Computer-Networks- Andrew S. Tanenbaum and David J. Wetherall, Pearson Education, 5th Edition. (www.pearsonhighered.com/tanenbaum)
2. Computer Networking A Top-Down Approach -James F. Kurose and Keith W. Ross Pearson Education 7th Edition.

Reference Books:

1. Behrouz A Forouzan, Data and Communications and Networking, Fifth Edition, McGraw Hill, Indian Edition
2. Larry L Peterson and Bruce S Davie, Computer Networks, fifth edition, ELSEVIER

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>
- VTU e-Shikshana Program

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Simulation of Personal area network, Home area network, achieve QoS etc.

Note: For the Simulation experiments modify the topology and parameters set for the experiment and take multiple rounds of reading and analyze the results available in log files. Plot necessary graphs and conclude using NS2. Installation procedure of the required software must be demonstrated, carried out in groups, and documented in the report. Non simulation programs can be implemented using Java.

VLSI Design		Semester	VI
Course Code	BUE602	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: - To understand the operation of MOS transistor, Scaling and Small Geometry Effects. - To study the Fabrication process, Layout design and Inverter cross section. - To provide the insights of MOSFET characteristics. - To understand the CMOS Inverter static characteristics. - To learn different techniques for dynamic circuits and low power consumption.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Chalk and Talk. - Power Presentation and Videos. - Flipped Classes. - Practice Sessions.			
Module-1 MOS Transistors, CMOS Logic: The inverter, The nand gate, Combinational Logic, TheNOR gate, Compound gates, Pass transistors and transmission gates, Tristates, Multiplexers, Latches and Flip-Flops. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication process, Layout design rules, Gate Layout, Stick diagrams. VLSI Design Flow: Design specification, Design entry, Functional simulation, Planning placement and routing, Timing simulation, Fusing/fabrication in to the chip. Fabrication, packaging, and testing. RBT Levels: L2,L3			
Module-2 MOS Transistors: The metal oxide semiconductor(MOS)structure, The MOS system under external bias, Structure and operation of MOS transistors(MOSFET),MOSFET current-voltage characteristics, MOSFET Scaling and Small-Geometry Effects (Full Scaling, Constant Voltage Scaling only), MOSFET Capacitances (Only Theory Part) RBT Levels: L3, L4			
Module-3 MOS Inverter: Static Characteristics: Introduction, Resistive-load inverter, Inverters with n-type MOSFET load, CMOS inverter. RBT Levels: L3, L4			
Module-4 Dynamic Logic Circuits: Introduction, Basic principles of Pass transistor circuits, Voltage Bootstrapping, Synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques, High Performance Dynamic CMOS Circuits (Domino CMOS Logic only) RBT Levels: L3,L4			
Module-5 Low-Power CMOS Logic Circuits: Introduction, Overview of power consumption, Low power design through voltage scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits. RBT Levels: L3, L4			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

CO1: Demonstrate understanding of MOS transistor, CMOS fabrication flow and Layout.

CO2: Analyze the Structure, Characteristics and operations of MOSFETs.

CO3: Interpret the MOSFET Scaling and Small Geometric effects.

CO4: Demonstrate static characteristics of Resistive load Inverter, Pass transistor and CMOS Inverter.

CO5: Apply the different dynamic circuit techniques and design low power through voltage scaling CMOS.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:**Books**

1. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
2. "CMOS Digital Integrated Circuits Analysis and Design"-Sung-Mo Kang, Yusuf Leblebici, 3rd Edition.

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quiz • Seminar • Assignments

INFORMATION THEORY AND CODING		Semester	VI
Course Code	BUE613A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source. - Study various source encoding algorithms. - Model discrete & continuous communication channels. - Study various error control coding algorithms.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer methods (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. - Use of Video/Animation to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. - Introduce Topics in manifold representations. - Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model of Information Sources, Entropy and Information rate of Markoff Sources.			
RBT Levels: L1,L2,L3			
Module-2			
Source Coding: Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI Encoding of the Source Output, Shannon's Encoding Algorithm Shannon Fano Encoding Algorithm, Huffman codes, Extended Huffman coding, Arithmetic Coding, Lempel – Ziv Algorithm.			
RBT Levels: L1,L2,L3			
Module-3			
Information Channels: Communication Channels, Channel Models, Channel Matrix, Joint probability Matrix, Binary Symmetric Channel, System Entropies, Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, Binary Erasure Channel, Muroga Theorem, Continuous Channels.			
RBT Levels: L1,L2,L3			
Module-4			
Error Control Coding: Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error Detection and Error Correction Capabilities of Linear Block Codes, Single Error Correcting hamming Codes, Table lookup Decoding using Standard Array.			
Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction			
RBT Levels: L1,L2,L3			
Module-5			
Some Important Cyclic Codes: Golay Codes, BCH Codes			
Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm)			
RBT Levels: L1,L2,L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

- C01.** Explain concept of Dependent & Independent Source, measure of information Entropy, Rate of Information & Order of a source
- C02.** Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
- C03.** Model the continuous and discrete communication channels using input, output and joint probabilities
- C04.** Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes.
- C05.** Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours)**.

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Digital and analog communication systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.
3. Information Theory and Coding, Muralidhar Kulkarni, K.S. Shivaprakasha, Wiley India Pvt. Ltd, 2015, ISBN:978-81-265-5305-1.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of digital communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, K.N.Haribhat, D.Ganesh Rao, Cengage Learning, 2017.

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes • Assignments • Seminars

ASIC DESIGN		Semester	VI
Course Code	BUE613B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - Recognize and differentiate between ASIC and PLD types across all modules. - Understand the complete ASIC design flow and utilize CAD tools effectively. - Explore programming technologies like Antifuse, Static RAM, EPROM, etc., relevant to ASIC and PLD design. - Examine various types of PLDs such as ROMs, EPROMs, FPGAs, etc., and their applications as discussed in the modules. - Gain insight into Full custom, Semi-custom, and Programmable ASICs, and understand the role of ASIC cell libraries throughout the design process.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lectures & Workshops 2. Labs & Case Studies 3. Group Discussions & Projects 4. Assessments			
Module-1			
Overview of ASIC and PLD: Types of ASICS Design Flow - CAD tools used in ASIC Design			
Programming Technologies: Antifuse-Static RAM - EPROM and EEPROM Technology, Programmable Logic Devices: ROMs and EPROMs - PLA - PAL. Gate Arrays - CPLDs and FPGAs			
RBT Levels: L1, L2			
Module-2			
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.			
CMOS Logic: Data path Logic Cells: Data Path Elements, Data path Operators, I/O cells, Cell Compilers.			
RBT Levels: L1, L2			
Module-3			
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design.			
Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block			
RBT Levels: L1, L2,L3			
Module-4			
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.			
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size.			
Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement,			
RBT Levels: L1, L2,L3			
Module-5			
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.			
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.			
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back- annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Special Routing, Circuit extraction and DRC.			
RBT Levels: L1, L2,L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

- CO 1:** Understand ASIC and PLD types, design flow, and CAD tools.
- CO 2:** Differentiate programming technologies and their applications.
- CO 3:** Evaluate ASIC types, design flows, and cell libraries.
- CO 4:** Apply logical effort principles for delay prediction and optimization.
- CO 5 :** Implement schematic entry, partitioning, floor planning, and routing techniques in ASIC design

Assessment Details (both CIE and SEE) :

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours)**.

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:**Textbook:**

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005

Reference:

1. "Digital Principles and Logic Design", A. Saha and N. Manna. (ISBN: 978-1-934015-03-2)
2. David A. Hodges, Analysis and Design of Digital Integrated Circuits, 3rd Edition, Tata Mc Graw Hill, 2004.
3. M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Group discussion and CAD tool demos for ASIC and PLD design flow understanding.
2. Interactive case studies and programming exercises for different programming technologies.
3. Role-playing as ASIC designers and comparative analysis of cell libraries.
4. Problem-solving sessions on delay prediction and optimization using logical effort principles.
5. Collaborative design projects and CAD tool workshops for floor planning, placement, and routing techniques.

DATA SCIENCE		Semester	VI
Course Code	BUE613C	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination Type (SEE)	Theory		
Course Objectives: • Demonstrate the proficiency with statistical analysis of data to derive insight from results and interpret the data findings visually. • Utilize the skills in data management by obtaining, cleaning and transforming the data. • Make use of machine learning models to solve the business-related challenges • Experiment with decision trees, neural network layers and data partition. • Demonstrate how social clustering shape individuals and groups in contemporary society.			
Teaching-Learning Process (General Instructions): These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer methods (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. 6. Introduce Topics in manifold representations. 7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Introduction: Visualizing Data, matplotlib, Bar Charts, Line Charts, Scatter plots, Linear Algebra, Vectors, Matrices, Statistics, Describing a Single Set of Data, Correlation, Simpson's Paradox, Some Other Correlational Caveats, Correlation and Causation, Probability, Dependence and Independence, Conditional Probability, Bayes's Theorem, Random Variables, Continuous Distributions, The Normal Distribution, The Central Limit Theorem. RBT Levels: L1, L2			
Module-2			
Hypothesis and Inference: Statistical Hypothesis Testing, Example: Flipping a Coin, p-Values, Confidence Intervals, p-Hacking, Example: Running an A/B Test, Bayesian Inference, Gradient Descent, The Idea Behind Gradient Descent Estimating the Gradient, Using the Gradient, Choosing the Right Step Size, Using Gradient Descent to Fit Models, Minibatch and Stochastic Gradient Descent, Getting Data, stdin and stdout, Reading Files, Scraping the Web, Using APIs, Example: Using the Twitter APIs, Working with Data, Exploring Data, Using NamedTuples, Data classes, Cleaning and Munging, Manipulating Data, Rescaling, An Aside: tqdm, Dimensionality Reduction. RBT Levels: L1, L2			
Module-3			
Machine Learning: What is Machine Learning?, Overfitting and Underfitting, Correctness, The Bias-Variance Tradeoff, Feature Extraction and Selection, k-Nearest Neighbors, Example: The Iris Dataset, The Curse of Dimensionality, Naive Bayes, A Really Dumb Spam Filter, A More Sophisticated Spam Filter, Implementation, Testing Model, Simple Linear Regression, Using Gradient Descent, Maximum Likelihood Estimation, Multiple Regression, Further Assumptions of the Least Squares Model, Fitting the Model, Interpreting the Model, Goodness of Fit, Digression: The Bootstrap, Standard Errors of Regression Coefficients, Regularization, Logistic Regression, The Problem, The Logistic Function, Applying the Model, Goodness of Fit, Support Vector Machines. RBT Levels: L1, L2, L3			

Module-4
Decision Trees: What Is a Decision Tree?, Entropy, The Entropy of a Partition, Creating a Decision Tree, Putting It All Together, Random Forests, Neural Networks, Perceptrons, Feed-Forward Neural Networks, Backpropagation, Example: Fizz Buzz, Deep Learning, The Tensor, The Layer Abstraction, The Linear Layer, Neural Networks as a Sequence of Layers, Loss and Optimization, Example: XOR Revisited, Other Activation Functions, Example: Fizz Buzz Revisited, Softmaxes and Cross-Entropy, Dropout, Example: MNIST, Saving and Loading Models, Clustering, The Idea, The Model, Example: Meetups, Choosing k, Example: Clustering Colors, Bottom-Up Hierarchical Clustering. RBT Levels: L1, L2, L3
Module-5
Natural Language Processing: Word Clouds, n-Gram Language Models, Grammars, An Aside: Gibbs Sampling, Topic Modeling, Word Vectors, Recurrent Neural Networks, Example: Using a Character-Level RNN, Network Analysis, Betweenness Centrality, Eigenvector Centrality, Directed Graphs and Page Rank, Recommender Systems, Manual Curation, Recommending What's Popular, User-Based Collaborative Filtering, Item Based Collaborative Filtering, Matrix Factorization. RBT Levels: L1, L2
Course Outcome (Course Skill Set): At the end of the course, the student will be able to : CO 1: Identify and demonstrate data using visualization tools. CO 2: Make use of Statistical hypothesis tests to choose the properties of data, curate and manipulate data. CO 3: Utilize the skills of machine learning algorithms and techniques and develop models. CO 4: Demonstrate the construction of decision tree and data partition using clustering. CO 5: Experiment with social network analysis and make use of natural language processing skills to develop data driven applications.
Assessment Details (both CIE and SEE): The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: - There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. - Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks - Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) - The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). - The question paper will have ten questions. Each question is set for 20 marks. - There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

3. The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.
Suggested Learning Resources: Text Books: 1. Joel Grus, “Data Science from Scratch”, 2nd Edition, O’Reilly Publications/Shroff Publishers and Distributors Pvt. Ltd., 2019. ISBN-13: 978-9352138326. Reference Books: 1. Emily Robinson and Jacqueline Nolis, “Build a Career in Data Science”, 1st Edition, Manning Publications, 2020. ISBN: 978-1617296246. 2. Aurelien Geron, “Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems”, 2nd Edition, O’Reilly Publications/Shroff Publishers and Distributors Pvt. Ltd., 2019. ISBN-13: 978-1492032649. 3. Francois Chollet, “Deep Learning with Python”, 1st Edition, Manning Publications, 2017. ISBN13: 978-1617294433. 4. Jeremy Howard and Sylvain Gugger, “Deep Learning for Coders with fastai and PyTorch”, 1st Edition, O’Reilly Publications/Shroff Publishers and Distributors Pvt. Ltd., 2020. ISBN-13: 978-1492045526. 5. Sebastian Raschka and Vahid Mirjalili, “Python Machine Learning: Machine Learning and Deep Learning with Python, scikit-learn, and TensorFlow 2”, 3rd Edition, Packt Publishing Limited, 2019. ISBN-13: 978-1789955750.
Web links and Video Lectures (e-Resources): • Using Python : https://www.python.org • R Programming : https://www.r-project.org/27092022 • Python for Natural Language Processing : https://www.nltk.org/book/ • Data set: https://archive.ics.uci.edu/ml/datasets.html • Data set : www.kaggle.com/ruiromanini/mtcars • https://nptel.ac.in/courses/106/106/106106179/ • https://nptel.ac.in/courses/106/106/106106212/ • http://nlp-iiit.vlabs.ac.in/List%20of%20experiments.html • https://onlinecourses.nptel.ac.in/noc21_cs69/preview • https://www.youtube.com/playlist?list=PLw5h0DiJ-9PCn4shW4X43FSjEqdBwc1Cn
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Real world problem solving - Applying the machine learning techniques and developing models • Quizzes • Assignments • Seminars

CRYPTOGRAPHY AND NETWORK SECURITY		Semester	VI
Course Code	BUE613D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - To enhance students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography, Ensuring Message Integrity and Authentication. - To equip students with a basic foundation of Network Security by delivering the basics of Transport Level Security, wireless network security and e-mail, Internet Protocol security			
Teaching-Learning Process (General Instructions) - Chalk and Talk Method - Power-point Presentation - Videos - Flipped class Technique			
Module-1			
Computer and Network Security Concepts: Computer Security Concepts, Security attacks, A Model for Network Security Introduction to Number Theory: The Euclidean Algorithm, Modular Arithmetic. Classical Encryption Techniques: Symmetric Cipher Model Cryptography, Substitution Techniques, RBT Levels: L1, L2, L3			
Module-2			
Block Ciphers and the Data Encryption Standard: Traditional Block Cipher Structure, The Data Encryption Standard. Advanced Encryption Standard: AES Structure, AES Transformation Functions. Public-Key Cryptography and RSA: Principles of Public-Key Cryptosystems, The RSA Algorithm Other Public-Key Cryptosystem: Diffie-Hellman key Exchange RBT Levels: L1, L2, L3			
Module-3			
Message Authentication Codes: Message Authentication Requirements, Message Authentication Function Cryptographic Hash Functions: Applications of Cryptographic Hash Functions, Secure Hash Algorithm(SHA) Digital Signatures: Digital Signatures RBT Levels: L1, L2, L3			
Module-4			
Transport-Level Security: Web Security Considerations, Secure, Transport Layer Security, HTTPS, Secure Shell (SSH) Wireless Network Security: Wireless Security, Mobile device Security, IEEE 802.11 Wireless LAN Security RBT Levels: L1, L2, L3			
Module-5			
Electronic Mail Security: Internet Mail Architecture, Email Threats and Comprehensive Email Security, S/MIME, Pretty Good Privacy IP: IP Security Overview, IP Security Policy, Encapsulating Security Payload, Internet key Exchange RBT Levels: L1, L2, L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

C01: Identify basic security attacks and explain traditional cryptographic algorithms of encryption and decryption process.

C02: Use symmetric and asymmetric key algorithms for cryptography.

C03: explain the need for message authentication, applications of cryptographic hash functions and explain the need of digital signatures.

C04: Analyze the vulnerabilities in any computing system and hence be able to design a security solution.

C05: Explain Security concerns in electronic-mail and Internet Protocol security

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:**Textbook:**

1. Cryptography and Network Security: Principles and Practice 7th Global Edition, Pearson Education Limited.

Reference Book:

2. Cryptography and Network Security – by Atul Kahate – TMH.
3. Behrouz A. Forouzan, Debdeep Mukhopadhyay, “Cryptography and Network Security”, Second edition, McGraw Hill Education

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz
- Seminar
- Assignment

FUNDAMENTALS OF EMBEDDED SYSTEMS		Semester	VI
Course Code	BUE654A	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
Course objectives: - Understand the basics of computer architecture and memory elements. - Introduce the general characteristics of embedded systems. - Bring the concepts related to microcontroller unit - Bring the interfacing concepts related to embedded systems .			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. - Use of Video/Animation to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.			
Module-1			
Basics of computer architecture and the binary number system Basics of computer architecture, computer languages, RISC and CISC architectures, number systems, number format conversions, computer arithmetic, units of memory capacity RBT Levels: L1, L2,L3			
Module-2			
Introduction to embedded systems Application domain of embedded systems, desirable features and general characteristics of embedded systems, model of an embedded system, microprocessor Vs microcontroller, example of a simple embedded system, figure of merit for an embedded system, classification of MCUs: 4/8/16/32 bits, history of embedded systems, current trends RBT Levels: L1, L2,L3			
Module-3			
Embedded systems -The hardware point of view Microcontroller unit(MCU), a popular 8-bit MCU, memory for embedded systems, low power design, pull up and pull down resistors RBT Levels: L1, L2,L3			
Module-4			
Sensors, ADCs and Actuators Sensors: Temperature Sensor, Light Sensor, Proximity/range Sensor; Analog to digital converters: ADC Interfacing; Actuators Displays, Motors, Opto couplers/Opto isolators, relays. RBT Levels: L1, L2,L3			
Module-5			
Examples of embedded systems Mobile phone, automotive electronics, radio frequency identification (RFID), wireless sensor networks(WISENET), robotics, biomedical applications, brain machine interface. RBT Levels: L1, L2,L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

- C01.** Learn about the general principles of computer architecture
- C02.** Learn about the working of a simple embedded system and its application.
- C03.** Learn the hardware aspects of embedded systems
- C04.** Understand the sensors, ADCs and actuators used in embedded systems.
- C05.** Understand the real world examples of embedded systems

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:**Textbooks:**

1. Lyla B Das, Embedded systems: An Integrated Approach, 1st Ed., Pearson, 2013

Reference Books:

1. Shibu, K.V., Introduction to Embedded Systems, 1st Ed., TMH, 2009
2. Kanta Rao B, Embedded Systems, 1st Ed., PHI
3. Frank Vahid & Tony Givargis, Embedded System Design, 2nd Edition, John Wiley,

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminar

Introduction to VLSI Circuits and Systems		Semester	VI
Course Code	BUE654B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - To learn Basic Concepts of VLSI. - To understand Basic Logic gates in CMOS. - To learn Physical Structure of CMOS Integrated Circuits. - To understand Design Rules of CMOS Integrated Circuits. - To learn Different types of Memories and Programmable Logic.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Chalk and Talk. - Power Presentation and Videos. - Flipped Classes. - Practical Sessions.			
Module-1			
An Overview of VLSI : Complexity and Design, Basic Concept Logic Design with MOSFETs: Ideal Switches and Boolean Operations, MOSFETs as Switches, Basic Logic Gates in CMOS. RBT Levels: L2			
Module-2			
Logic Design with MOSFETs: Complex Logic Gates in CMOS, Transmission Gate Circuits, Physical Structure of CMOS Integrated Circuits: Integrated Circuit Layers, MOSFETs: nFETs and pFETs, Current Flow in a FET, Driving the Gate Capacitance RBT Levels: L1,L2			
Module-3			
Physical Structure of CMOS Integrated Circuits: CMOS Layers, Designing FET Arrays. Electrical Characteristics of MOSFETs: MOS Physics, nFET Current-Voltage Equations. RBT Levels:,L3			
Module-4			
Electrical Characteristics of MOSFETs: The FET RC Mode, pFET Characteristics, Modelling of Small MOSFETs. Electronic Analysis of CMOS Logic Gates: DC Characteristics of the CMOS Inverter, Inverter switching Characteristics RBT Levels: L3,L4			
Module-5			
Electronic Analysis of CMOS Logic Gates: Power Dissipation, DC Characteristics: NAND and NOR Gates,NAND and NOR Transient Response, Analysis of Complex Logic Gates, Gate Design for Transient Performance, Transmission Gates and Pass Transistors. RBT Levels: L4			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

C01.Demonstrate understanding of Logic design with MOSFET.

C02.Analyze various Integrated Circuit Layers.

C03.Interpret the Designing of FET Arrays and Basic gates design.

C04. Interpret the CMOS Process Flow and Design Rules.

C05.Demonstrate knowledge of Memories and Programmable Logic Array.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:**Books**

1. John P. Uyemura " Introduction to VLSI Circuits and Systems"

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective" - Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.

Web links and Video Lectures (e-Resources):

- http://vlsipd1.blogspot.com/?trk=article-ssr-frontend-pulse_little-text-block
- https://vlsipd.blogspot.com/?trk=article-ssr-frontend-pulse_little-text-block
- https://www.youtube.com/redirect?event=video_description&redir_token=QUFFLUhqa202NTRGQ1FnVXM0SXg0UGxxV1ZQV1U1TVB5UXxBQ3Jtc0trUE5RM1FvWEINOHdaY1NtMWtkek8wWGdGMV80aEFjRHRaWko4X3pnNTcxX0FjRXNfUnY3eE9GUG5FMlp0NDluajhOVkV2V2V0SU0wWjA3UXFEQUFBR1BNM2tnYXIWZHIjCTi1leVBxMUhPQUlzc1UUQ&q=http%3A%2F%2FnpTEL.iitm.ac.in%2F&v=Abld-fSxjNM

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminars

MICROPROCESSORS AND MICROCONTROLLERS		Semester	VI
Course Code	BUE654C	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
Course objectives: 1. To learn the design aspects of I/O and Memory Interfacing circuits. 2. To Study about communication and bus interfacing. 3. To Study the Architecture of 8051 microcontroller. 4. To get exposed to RISC processors and design ARM microcontroller-based systems			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.			
Module-1			
8085 MICROPROCESSOR: Microprocessor architecture and its operation, memory, I/O devices, 8085 microprocessor – Core architecture - Various registers- Bus Timings, Multiplexing and Demultiplexing of Address Bus, Decoding and Execution, Instruction set – Classification, Instruction Format, Addressing Modes, 8085 Interrupt Process, Hardware and Software Interrupts. RBT Levels: L1,L2			
Module-2			
8086 MICROPROCESSOR: Core Architecture of the 8086 - Memory Segmentation, Minimum mode Operation and Maximum Mode Operation, Instruction Set of the 8086 processor- Classification - Instruction Format Addressing modes, Simple Assembly Language Programs - Arithmetic operations, Data transfer, String Manipulation, Searching and Sorting . RBT Levels: L1,L2			
Module-3			
I/O INTERFACING: Memory Interfacing and I/O interfacing - Parallel communication interface – Serial Communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller. RBT Levels: L2,L3			
Module-4			
MICROCONTROLLER: Architecture of 8051 – Special Function Registers (SFRs) - I/O Pins Ports and Circuits – Instruction set- Addressing modes - Assembly language programming - Programming 8051 Timers, Serial Port Programming - Interrupts Programming – LCD & Keyboard Interfacing - ADC, DAC & Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation. RBT Levels: L1,L2			
Module-5			
ADVANCED MICROPROCESSOR & MICROCONTROLLER: Advanced coprocessor Architectures- 286, 486, Pentium -RISC Processors- RISC Vs CISC, RISC properties and evolution- ARM Processor – CPU: programming input and output supervisor mode, exceptions and traps – Co-processors, Memory system mechanisms – CPU			

performance- CPU power consumption.

RBT Levels: L2,L3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Design interfacing peripherals like, I/O, A/D, D/A, timer etc.
2. Develop systems using different microcontrollers.
3. Characterize RISC processors and design ARM microcontroller-based systems

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Textbooks:

1. R. S. Gaonkar, "Microprocessor Architecture: Programming and Applications with the 8085/8080A", Penram International Publishing, Third Edition, 1996.
2. D A Patterson and J H Hennessy, "Computer Organization and Design The hardware and software interface" Morgan Kaufman Publishers, Fourth Edition, 2011.
3. Douglas Hall, "The Microprocessors and its Interfacing", Tata McGraw Hill, Third Edition, 2012.
4. Kenneth J. Ayala, "The 8051 Microcontroller: Architecture Programming & Applications", Penram International Publishing, Second Edition, 1996.
5. Yu-Cheng Liu, Glenn A. Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2011.
6. Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and

Embedded Systems: Using Assembly and C”, Second Edition, Pearson education, 2011.	
2. Reference Books:	
1. Douglas V. Hall, “Microprocessors and Interfacing, Programming and Hardware”, Second Edition, TMH, 2012. 2. John P. Hayes, “Computer Architecture and Organization”, Third illustrated Edition, Tata McGraw Hill, 2007.	
Web links and Video Lectures (e-Resources):	
• https://nptel.ac.in/	
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning	
• Quizzes • Seminar	

ELECTRONIC INSTRUMENTATION		Semester	VI
Course Code	BUE654D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - Define and describe accuracy and precision, and types of errors. - Describe the operation of Ammeters, Voltmeters and Multi-meters and develop circuits for multi range Ammeters and Voltmeters. - Describe functional concepts and operation of various Analog and Digital measuring instruments. - Describe basic concepts and operation of Digital Voltmeters. - Describe and discuss the functioning and types of Oscilloscopes, Signal generators, AC and DC bridges. - Recognize and describe the significance and working of different types of transducers.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. - Use of Video/Animation to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.			
Module-1			
Measurement and Error: Definitions, Accuracy, Precision, Resolution and Significant Figures, Types of Errors, Measurement error combinations. Ammeters: DC Ammeter, Multi range Ammeter, The Ayrton Shunt or Universal Shunt, Requirements of Shunt, Extending of Ammeter Ranges, RF Ammeter (Thermocouple), Limitations of Thermocouple. Voltmeters and Multi-meters: Introduction, Basic Meter as a DC Voltmeter, DC Voltmeter, Multi range Voltmeter, Extending Voltmeter Ranges, Loading, AC Voltmeter using Rectifiers. True RMS Voltmeter, Multirange Voltmeter. RBT Levels: L1,L2,L3			
Module-2			
Digital Voltmeters: Introduction, RAMP technique, Dual Slope Integrating Type DVM, Integrating Type DVM, Most Commonly used principles of A DC, Successive Approximations, Resolution and Sensitivity of Digital Meters, General Specifications of DVM Digital Instruments: Introduction, Digital Multimeters, Digital Frequency Meter, Digital Measurement of Time, Universal Counter, Digital Tachometer, Digital pH Meter, Digital Phase Meter, Digital Capacitance Meter. RBT Levels: L1,L2,L3			
Module-3			
Oscilloscopes: Introduction, Basic principles, CRT features, Block diagram of Oscilloscope, Simple CRO, Measurement of Frequency by Lissajous Method, Digital Storage Oscilloscope. Signal Generators: Introduction, Fixed and Variable AF Oscillator, Standard Signal Generator, Laboratory Type Signal Generator, AF sine and Square Wave Generator, Function Generator. RBT Levels: L1,L2			
Module-4			
Measuring Instruments: Field Strength Meter, Stroboscope, Phase Meter, Q Meter, Megger. Bridges: Introduction, Wheatstone's bridge, Kelvin's Bridge; AC bridges, Capacitance Comparison Bridge, Inductance Comparison Bridge, Wien's bridge. RBT Levels: L1,L2,L3			
Module-5			

Transducers: Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance the rmo meter, Thermistor, Inductive transducer, LVDT, Piezo electric transducer, Photo voltaic cell, Semiconductor photo diode and transistor

RBT Levels: L1,L2,L3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

- CO1.**Describe instrument measurement errors and calculate them.
- CO2.**Describe the operation of Ammeters, Voltmeters, Multi-meters & develop circuits for multi range Ammeters and Voltmeters.
- CO3.**Describe functional concepts and operation of Digital voltmeters and instruments to measure voltage, frequency, time period, phase difference of signals, rotation speed, capacitance and pH of solutions.
- CO4.**Describe functional concepts and operation of various Analog measuring instruments to measure field Strength, impedance, stroboscopic speed, in/out of phase, Q of coils, insulation resistance.
- CO5.**Describe and discuss functioning and types of Oscilloscopes, Signal generators and Transducers.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored shall be proportionally reduced to 50 marks.
Suggested Learning Resources: Text Books: 1. H.S. Kalsi, - Electronic Instrumentation , McGraw Hill, 3rd Edition, 2012, ISBN:9780070702066. 2. David A. Bell, —Electronic Instrumentation & Measurements , Oxford University Press PHI 2nd Edition, 2006, ISBN81-203-2360-2 Reference Books: 1. A. D. Helfrick and W. D. Cooper — Modern Electronic Instrumentation and Measuring Technique, Pearson, 1st Edition, 2015, ISBN:9789332556065. 2. A.K.Sawhney, —Electronics and Electrical Measurement, Dhanpat Rai & Sons, ISBN-81-7700-016-0
Web links and Video Lectures (e-Resources): • https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes • Seminars • Assignments

VLSI Laboratory		Semester	VI
Course Code	BUEL606	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
Total Hours of Pedagogy	12-14 slots	Exam Hours	2 Hours
Examination type (SEE)	Practical		
Course objectives: - To verify the LVS, DRC, ERC parameters for designed layouts. - Understand the features of CAD tool in VLSI design. - To learn the fundamental principles of VLSI circuit design in digital domain. - Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list			
Sl.NO	Experiments		
PART A : ASIC-Digital Design Flow <i>(Experiments to be conducted using any suitable CAD tool)</i>			
Write the Verilog Code and their Test Bench for the following circuits. Observe the waveform, Synthesize the code, do the initial timing verification with gate level simulation.			
1	4 -Bit Ripple Carry Adder		
2	4-Bit Booth Multiplier		
3	a) LFSR b) Parity generators		
4	Master Slave JK Flip Flop		
5	4-Bit Ring Counter		
6	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations		
PART B : Analog VLSI Design <i>(Experiments to be conducted using any suitable CAD tool)</i>			
Draw the Schematic and Layout for the circuits mentioned below with the help of Suitable CAD tool and verify the following. a. Schematic: i) DC Analysis ii) Transient Analysis iii) Parametric analysis b. Layout: i) DRC ii) LVS iii) RC Extraction and Back Annotation.			
7	CMOS Inverter		
8	CMOS two input NAND		
9	a) Common Source Amplifier b) Common Drain Amplifier		
10	Current Mirror Circuit		
Demonstration Experiments (For CIE)			
11	Design a 4 bit R-2R based DAC		

12	Design and characterize 3T DRAM cell and measure the following: • Read Time, Write Time, Power • Draw Layout of 3T DRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, Record the observations.
Course outcomes (Course Skill Set): At the end of the course the student will be able to: C01. Understand the physical design process of Digital Integrated Circuits. C02. Implement various combinational and sequential circuits using HDL. C03. Implement schematic and layout of various digital CMOS logic circuits using EDA tools. C04. Describe procedure for designing of programmable circuits.	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation (CIE): CIE marks for the practical course are 50 Marks. The split-up of CIE marks for record/ journal and test are in the ratio 60:40. • Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session. • Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks. • Total marks scored by the students are scaled down to 30 marks (60% of maximum marks). • Weightage to be given for neatness and submission of record/write-up on time. • Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus. • In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.	
Semester End Evaluation (SEE): • SEE marks for the practical course are 50 Marks. • SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university. • The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University. • All laboratory experiments are to be included for practical examination. • (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners. • Students can pick one question (experiment) from the questions lot prepared by the examiners jointly. • Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)	

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

<https://nptel.ac.in/>

Reference book :

Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog 1st Edition, Kindle Edition

LATEX SOFTWARE		Semester	VI																											
Course Code	BUE657A	CIE Marks	50																											
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50																											
Credits	01	Total SEE+CIE	100																											
Total Hours of Pedagogy	12-14 slots	Exam Hours	2 Hours																											
Examination type (SEE)	Practical																													
Course objectives: - To introduce the basic syntax and semantics of the LaTeX scripting language - To understand the presentation of tables and figures in the document - To illustrate the LaTeX syntax to represent the theorems and mathematical equations - To make use of the libraries (Tikz, algorithm) to design the diagram and algorithms in the document																														
Sl. NO	Experiments																													
1	Develop a LaTeX script to create a simple document that consists of 2 sections [Section1, Section2], and a paragraph with dummy text in each section. And also include header [title of document] and footer [institute name, page number] in the document.																													
2	Develop a LaTeX script to create a document that displays the sample Abstract/Summary																													
3	Develop a LaTeX script to create a simple title page of the VTU project Report [Use suitable Logos and text formatting]																													
4	Develop a LaTeX script to create the Certificate Page of the Report [Use suitable commands to leave the blank spaces for user entry]																													
5	Develop a LaTeX script to create a document that contains the following table with proper labels. <table><tr><th rowspan="2">S.No</th><th rowspan="2">USN</th><th rowspan="2">Student Name</th><th colspan="3">Marks</th></tr><tr><th>Subject1</th><th>Subject2</th><th>Subject3</th></tr><tr><td>1</td><td>4XX22XX001</td><td>Name 1</td><td>89</td><td>60</td><td>90</td></tr><tr><td>2</td><td>4XX22XX002</td><td>Name 2</td><td>78</td><td>45</td><td>98</td></tr><tr><td>3</td><td>4XX22XX003</td><td>Name 3</td><td>67</td><td>55</td><td>59</td></tr></table>			S.No	USN	Student Name	Marks			Subject1	Subject2	Subject3	1	4XX22XX001	Name 1	89	60	90	2	4XX22XX002	Name 2	78	45	98	3	4XX22XX003	Name 3	67	55	59
S.No	USN	Student Name	Marks																											
			Subject1	Subject2	Subject3																									
1	4XX22XX001	Name 1	89	60	90																									
2	4XX22XX002	Name 2	78	45	98																									
3	4XX22XX003	Name 3	67	55	59																									
6	Develop a LaTeX script to include the side-by-side graphics/pictures/figures in the document by using the subgraph concept																													
7	Develop a LaTeX script to create a document that consists of the following two mathematical equations $x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$= \frac{-2 \pm \sqrt{2^2 - 4*(1)*(-8)}}{2*1}$$= \frac{-2 \pm \sqrt{4+32}}{2}$ $\varphi_{\sigma}^{\lambda} A_t = \sum_{\pi \in C_t} \text{sgn}(\pi) \varphi_{\sigma}^{\lambda} \varphi_{\pi}^{\lambda}$$= \sum_{\tau \in C_{\sigma t}} \text{sgn}(\sigma^{-1} \tau \sigma) \varphi_{\sigma}^{\lambda} \varphi_{\sigma^{-1} \tau \sigma}^{\lambda}$$= A_{\sigma t} \varphi_{\sigma}^{\lambda}$																													
8	Develop a LaTeX script to demonstrate the presentation of Numbered theorems, definitions, corollaries, and lemmas in the document																													
	Demonstration Experiments (For CIE)																													
9	Develop a LaTeX script to create a document that consists of two paragraphs with a minimum of 10 citations in it and display the reference in the section																													

10	Develop a LaTeX script to design a simple tree diagram or hierarchical structure in the document with appropriate labels using the Tikz library
11	Develop a LaTeX script to present an algorithm in the document using algorithm/algorithmic/algorithm2e library
12	Develop a LaTeX script to create a simple report and article by using suitable commands and formats of user choice.
Course outcomes (Course Skill Set): At the end of the course the student will be able to: C01. Apply basic LaTeX command to develop simple document C02. Develop LaTeX script to present the tables and figures in the document C03. Illustrate LaTeX script to present theorems and mathematical equations in the document C04. Develop programs to generate the complete report with citations and a bibliography C05. Illustrate the use of Tikz and algorithm libraries to design graphics& algorithms in the document	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation (CIE): CIE marks for the practical course are 50 Marks. The split-up of CIE marks for record/ journal and test are in the ratio 60:40. • Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session. • Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks. • Total marks scored by the students are scaled down to 30 marks (60% of maximum marks). • Weightage to be given for neatness and submission of record/write-up on time. • Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus. • In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce. • The suitable rubrics can be designed to evaluate each student's performance and learning ability. • The marks scored shall be scaled down to 20 marks (40% of the maximum marks). The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.	
Semester End Evaluation (SEE): • SEE marks for the practical course are 50 Marks. • SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university. • The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University. • All laboratory experiments are to be included for practical examination. • (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be	

strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

BOOK:

1. A Short Introduction to LaTeX BY FIRUZA KARMALI (AIBARA), A book for beginners,2019
2. Formatting Information: A Beginner's Introduction to Typesetting with LaTeX, BY PETERFLYNN, Comprehensive TeX Archive Network (2005)

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Seminars
- Assignments

APTITUDE VERBAL NUMERICAL AND LOGICAL REASONING		Semester	VI
Course Code	BUE657B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	01	Exam Hours	1 Hour
Examination type (SEE)	MCQ		
Course objectives: - To make the students aware of the importance of Aptitude in the present-day Competitive exams . - To train the students develop the required skills to think in new and innovative way. - To develop basic Aptitude knowledge to understand advanced concept in higher semester.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it. - Introduce Topics in manifold representations. - Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. - Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Aptitude Verbal: Reading/Comprehension, Sentence Completion (Vocabulary), Sentence Completion (Subject-Verb Agreement), Sentence Completion (Tenses)			
RBT Levels: L1,L2,L3			
Module-2			
Quantitative Ability (Applied & Engineering Mathematics): Logarithm, Permutation and Combinations, Probability, Simple and Compound Interest, Quick Calculation of Percentages, Conversion of Fraction to Percentage Table, Successive Percentage, Concept of 'By' & 'To', Percentage Change, Percentage Point Change, Product Constancy, Increased Value & Increase in Value, Percentage Changes in Numerator & Denominator, Successive Percentage			
RBT Levels: L1,L2,L3			
Module-3			
Quantitative Ability (Applied & Engineering Mathematics): Time, Speed and Distance Time & Work, Ratio and Proportion Duplicate Ratio, Triplicate Ratio, Direct Proportion, Indirect Proportion, Double rule of three or compound proportion, Ratio in investment or partnership, Area			
RBT Levels: L1,L2,L3			
Module-4			
Data Interpretation: Data Interpretation, Tables, Column Graphs, Bar Graphs, Line Charts, Pie Chart, Venn Diagrams Profit, Loss, Cost Price, Selling Price, Marked Price			
RBT Levels: L1,L2,L3			
Module-5			
Logical Reasoning (Deductive Reasoning): Analogy, Blood Relation Relations defined, Generation Verticals, Family Tree, Single Person Blood Relations, Mixed/Chain Blood Relations, Symbol based Blood Relation, Directional Sense, Number and Letter Series, Coding – Decoding, Calendars			
RBT Levels: L1,L2,L3			

Course outcome (Course Skill Set) At the end of the course the student will be able to: CO1. Understand the basic concepts of quantitative ability. CO2. Understand the basic concepts of logical reasoning Skills. CO3. Acquire satisfactory competency in use of reasoning. CO4. Solve campus placements aptitude papers covering Quantitative & Logical Reasoning Ability. CO5. Compete in various competitive exams like CAT, CMAT, GATE, GRE, GATE, UPSC, GPSC etc.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous internal Examination (CIE) - For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks. - The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered - Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. - For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester End Examinations (SEE) SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.
Suggested Learning Resources: Text Books 1. A Modern Approach To Verbal & Non Verbal Reasoning By R S Agarwal 2. Analytical and Logical reasoning By Sijwali B S 3. Quantitative aptitude for Competitive examination By R S Agarwal 4. Analytical and Logical reasoning for CAT and other management entrance test By Sijwali B S 5. Quantitative Aptitude by Competitive Examinations by Abhijit Guha 4 th edition 6. Dr.Ravi Chopra – “Verbal and Non-Verbal Reasoning”, MacMillan India
Web links and Video Lectures (e-Resources): • https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes • Seminars • Assignments

WEB PROGRAMMING (Practical based)			
Course Code	BUEL657D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Total Hours of Pedagogy	12T + 12P	Total Marks	100
Credits	01	Exam Hours	02
Course Objectives: CLO 1. Learn Web tool box and history of web browsers. CLO 2. Learn HTML, XHTML tags with utilizations. CLO 3. Know CSS with dynamic document utilizations. CLO 4. Learn JavaScript with Element access in JavaScript. CLO 5. Logically plan and develop web pages..			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) needs not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. 6. Introduce Topics in manifold representations. 7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Introduction to WEB Programming: Internet, WWW, Web Browsers, and Web Servers, URLs, MIME, HTTP, Security, The Web Programmers Toolbox.			
Teaching-Learning Process	Chalk and board, Active Learning, practical based learning		
Module-2			
HTML and XHTML: Origins of HTML and XHTML, Basic syntax, Standard XHTML document structure, Basic text markup, Images, Hypertext Links, Lists, Tables. Forms, Frames in HTML and XHTML, Syntactic differences between HTML and XHTML.			

Teaching-Learning Process	Chalk and board, Active Learning, Demonstration, presentation, problem solving
Module-3	
CSS: Introduction, Levels of style sheets, Style specification formats, Selector forms, Property value forms, Font properties, List properties, Color, Alignment of text, Background images, tags.	
Teaching-Learning Process	Chalk and board, Demonstration, problem solving
Module-4	
Java Script – I: Object orientation and JavaScript; General syntactic characteristics; Primitives, Operations, and expressions; Screen output and keyboard input.	
Teaching-Learning Process	Chalk and board, Practical based learning, practical's
Module-5	
Java Script – II: Control statements, Object creation and Modification; Arrays; Functions; Constructor; Pattern matching using expressions; Errors, Element access in JavaScript.	
Teaching-Learning Process	Chalk and board, MOOC
Course Outcomes (Course Skill Set): At the end of the course the student will be able to: CO 1. Describe the fundamentals of web and concept of HTML. CO 2. Use the concepts of HTML, XHTML to construct the web pages. CO 3. Interpret CSS for dynamic documents. CO 4. Evaluate different concepts of JavaScript & Construct dynamic documents. CO 5. Design a small project with JavaScript and XHTML.	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE). Continuous Internal Evaluation (CIE): <i>NOTE: List of experiments to be prepared by the faculty based on the syllabus mentioned above</i> CIE marks for the practical course is 50 Marks . The split-up of CIE marks for record/ journal and test are in the ratio 60:40 . - Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session. - Record should contain all the specified experiments in the syllabus and each	

experiment write-up will be evaluated for 10 marks.

- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are
Appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedules mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- The duration of SEE is 02 hours

Rubrics suggested in Annexure-II of Regulation book

Textbooks

1. Robert W Sebesta, "Programming the World Wide Web", 6th Edition, Pearson Education, 2008.

Reference Books

1. M.Deitel, P.J.Deitel, A.B.Goldberg, "Internet & World Wide Web How to program", 3rd Edition, Pearson Education / PHI, 2004.

2. Chris Bates, "Web Programming Building Internet Applications", 3rd Edition, Wiley India,

2006.

3. Xue Bai et al, "The Web Warrior Guide to Web Programming", Thomson, 2003.

4. Sklar, "The Web Warrior Guide to Web Design Technologies", 1st Edition, Cengage Learning India

Weblinks and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Demonstration of simple projects

ADVANCED PYTHON PROGRAMMING		Semester	VI
Course Code	BUEL657C	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination Type (SEE)	Practical		
Course Objectives: • Demonstrate the use of IDLE or PyCharm IDE to create Python Applications. • Using Python programming language to develop programs for solving real-world problems • Implementation of Matplotlib, Seaborn, Bokeh and Plotly for drawing different Plots. • Demonstrate working with Numpy, Pandas libraries and creation of GUI.			
Sl. No.	Experiments		
1	a) Write a Python program to Demonstrate how to Draw a Bar Plot using Matplotlib. b) Write a Python program to Demonstrate how to Draw a Scatter Plot using Matplotlib.		
2	a) Write a Python program to Demonstrate how to Draw a Histogram Plot using Matplotlib. b) Write a Python program to Demonstrate how to Draw a Pie Chart using Matplotlib.		
3	a) Write a Python program to illustrate Linear Plotting using Matplotlib. b) Write a Python program to illustrate liner plotting with line formatting using Matplotlib.		
4	Write a Python program to perform the following basic operations on an image: (i) Crop (ii) Scale (iii) Rotate (iv) Flip.		
5	Write a Python program to perform the following operations on an image: (i) Changing contrast and brightness (ii) Edge detection, blur, sharpening.		
6	Write a Python program to perform basic numerical processing using Numpy.		
7	Write a Python program to create a GUI using Widgets.		
8	Write a Python program to perform the following operations using Pandas: (i) Loading a dataset into a dataframe (ii) Selecting Columns from a dataframe (iii) Selecting Rows from a dataframe (iv) Adding new data in a dataframe (v) Deleting data from a dataframe.		
	Demonstration Experiments (For CIE)		
9	Write a Python program to explain working with bokeh line graph using Annotations and Legends.		
10	Write a Python program to draw 3D Plots using Plotly Libraries.		
11	Write a Python program to perform following operations on images: a) Addition of two images b) Subtraction of two images		
12	Write a Python program to detect different Facial features.		

Course Outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO 1: Demonstrate the use of IDLE or PyCharm IDE to create Python Applications.

CO 2: Use Python programming constructs to develop programs for solving real-world problems.

CO 3: Use Matplotlib, Seaborn, Bokeh and Plotly for drawing different Plots for visualization.

CO 4: Demonstrate working with Numpy, Pandas libraries and creation of GUI.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be

scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

Textbooks:

1. Al Sweigart, "Automate the Boring Stuff with Python", 1st Edition, No Starch Press, 2015.
2. Reema Thareja "Python Programming Using Problem Solving Approach" Oxford University Press.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Seminars
- Assignments

Semester - VII

PRINCIPLES OF AI and ML			
Course Code	BUE701	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Course objectives: - To understand the main approaches to Artificial intelligence, Machine learning - To Analyse and interpret data using AI techniques. - To Design and implement AI-powered applications that meet specific requirements.			
MODULE-1			
Introduction to Artificial Intelligence: Introduction, what is AI, Strong Methods and weak Methods. Uses and Limitations: Knowledge Representation: Need for good representation, semantic nets, Frames, , Search Spaces, Semantics Tress, Search Trees, Combinatorial Explosion, Problem reduction, Goal Trees, Combinatorial Explosion. RBT Levels: L1, L2			
MODULE-2			
Search Methodologies: Introduction, Problem solving as search, Data driven or goal driven search, Generate and test, Properties of search methods, Depth First Iterative Deepening, Using Heuristics for Search, Hill Climbing, Best-First Search, Identifying Optimal Paths, Constraint Satisfaction search, Forward Checking, Local Search and Meta heuristics, Simulated Annealing. Genetic Algorithms for search, Real time A*, Bidirectional search, Nondeterministic search, non-chronological backtracking. RBT Levels: L1, L2			
MODULE-3			
Game Playing: Game Trees, Minimax, Alpha beta pruning. Propositional and Predicate Logic: Introduction, what is Logic, Why Logic is used in Artificial Intelligence, Logical Operators, translating between English and Logic Notation, The deduction Theorem, Soundness, Completeness, Decidability, Monotonicity, Abduction and Inductive reasoning, Modal logics and possible worlds, Dealing with change. Inference and Resolution for Problem Solving: Introduction, Resolution in prepositional logic: Applications of Resolution, Resolution in Predicate Logic, Normal forms for predicate logic, Skolemization, Resolution Algorithms, Resolution for problem solving. RBT Levels: L2, L3			
MODULE-4			
Introduction to Machine Learning: Introduction, Training Rote Learning, Learning Concepts, General-to-Specific Ordering, Version Spaces, Candidate Elimination, Inductive Bias, Decision-Tree Induction, The Problem of Overfitting, The Nearest Neighbor Algorithm, Backpropagation algorithms, Reinforcement Learning. Neural Networks: Introduction, Neurons, Perceptrons, Multilayer Neural Networks, Recurrent Networks, Unsupervised Learning Networks, Evolving Neural Networks. RBT Levels: L2, L3			
MODULE 5			
Probabilistic Reasoning and Bayesian Belief Networks: Introduction, Probabilistic Reasoning, Joint Probability Distributions, Bayes' Theorem, Simple Bayesian Concept Learning, Bayesian Belief Networks, The Noisy-V Function, Bayes' Optimal Classifier, The Naïve Bayes Classifier. RBT Levels: L2, L3			

PRACTICAL COMPONENT OF IPCC (May cover all / major modules)

Sl. No.	Experiments
1	Implement DFID algorithm and compare its performance with DFS and BFS algorithm
2	Implement Best-First Search algorithm
3	Implementation of AND/OR/NOT Gate using single layer perceptron.
4	Implementation of XOR Gate using a) Multi-layer perceptron/Error back propagation b) Radial Basis Function Network
5	Implement Hebbian learning rule and Correlation learning rule.
6	Implement Find-S and candidate elimination algorithms.
7	Build a linear regression model housing prices.
8	Implement spam detection using Naïve Bayes Algorithm.
9	Implement hand writing classification using Support Vector Machines.
10	Implement FP-tree for finding co-occurring words in a twitter feed.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC:

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC:

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.

- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks-25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Text Books

1. Ben Coppin, Artificial Intelligence Illuminated, Jones and Bartlett, 2004.
2. Tom M. Mitchell, "Machine Learning", McGraw-Hill Education (Indian Edition), 2013.

Reference Books

1. Elaine Rich Kevin Knight, Shivashankar B Nair: Artificial Intelligence, Tata McGraw Hill 3rd edition 2013.
2. Stuart Russel, Peter Norvig: Artificial Intelligence A Modern Approach, Pearson 3rd edition 2013.
3. Ethem Alpaydin, "Introduction to Machine Learning", 2nd Edition, PHI Learning Pvt. Ltd., 2013.
4. T Hastie, R. Tibshirani, J.H.Fiedman, "The Elements of statistical learning", Springer, 1st Edition 2001.

Web links and Video Lectures (e-Resources):

- **Kaggle:** <https://www.kaggle.com/>
- **OpenAI:** <https://openai.com/>
- **TensorFlow:** <https://www.tensorflow.org/>
- **Scikit-learn:** <https://scikit-learn.org/>
- **Keras:** <https://keras.io/>
- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Create a debate on the ethical implications of strong AI.
- Implement different search algorithms to solve classic AI problems like the 8-puzzle or the traveling salesman problem.
- Build a simple machine learning model using a drag-and-drop interface.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
C01	Students will be able to explain the limitations and challenges associated with AI techniques.	2
C02	Students will be able to apply AI concepts to solve real-world problems, such as game playing, problem-solving using search algorithms, and building intelligent systems.	3
C03	Students will be able to analyse the strengths and weaknesses of different AI approaches and choose the most appropriate method for a given task.	4

Semester - VII

SystemVerilog			
Course Code	BUE702	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Course objectives: - Understand Digital System Verification Using Object Oriented Methods - Learn the System Verilog Language for Digital System Verification. - Create/Build Test Benches for the Design/Methodology. - Use Constrained Random Tests for Verification - Understand Concepts of Functional Coverage.			
MODULE-1			
Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench. Data Types: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With typedef, Creating User Defined Structures, Type Conversion, EnumeratedTypes, Constants and Strings, Expression Width. RBT Levels: L2, L3			
MODULE-2			
Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values. Connecting the Test Bench and Design: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions. RBT Levels: L2, L3			
MODULE-3			
Randomization: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, InLine Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators. RBT Levels: L3			
MODULE-4			
Threads and Inter process Communication: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, Building A Test Bench with Threads and InterProcess Communication. RBT Levels: L3			
MODULE 5			
Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, MeasuringCoverage Statistics During Simulation. RBT Levels: L3, L4			

PRACTICAL COMPONENT OF IPCC (May cover all / major modules)

Sl. No.	Experiments
1	(a) Write a SV code to demonstrate 2-state and 4-state data types. (b) Write a SV code to demonstrate the difference between bit and byte. (c) Write a SV code to demonstrate the difference between int and integer.
2	(a) Write a SV code to demonstrate for and foreach loops for multidimensional arrays. (b) Write a SV code to demonstrate packed and unpacked array.
3	(a) Write a SV code to implement a module to store and display a list of student grades using a dynamic array. (b) Develop a module that maps product names to their prices using associative array.

	(c) Write a SV code to demonstrate all the Queue operations.
4	(a) Write a SV code to demonstrate break and continue statements. (b) Develop a module to demonstrate Tasks, Functions and Void Function.
5	(a) Write a SV code to demonstrate rand and randc with random class. (b) Write a constraint for removing duplicate elements from queue. (c) Write a constraint to generate even numbers between 10 to 30.
6	(a) Write a constraint to arrange the initial numbers in ascending order and remaining numbers in descending order. (b) Write a constraint to generate a sequence of 9 99 999 9999 99999.
7	(a) Write a constraint to generate: • A queue with unique value. • Store a even number at the index of the odd value. • Store a odd number at the index of the even value. (b) Write a constraint to generate a pattern of 000111222333444555.
8	(a) Demonstrate fork-join, for-join-any, fork-join-none using suitable SV code. (b) Develop module of the mailbox connecting two transactors.
9	Demo Experiment - Demonstrate complete SV design that incorporates the entire SystemVerilog environment for simple digital circuit.
10	Demo Experiment - Demonstrate simple protocol through the SV environment.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC:

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 220B4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC:

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of

IPCC for **25 marks**.

- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks-25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Interact with industry (small, medium, and large).
- Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
- Involve in case studies and field visits/ fieldwork.
- Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
- Handle advanced instruments to enhance technical talent.
- Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
- Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Apply the SystemVerilog concepts to verify the design.	L3
CO2	Apply constrained random tests benches using SystemVerilog.	L3
CO3	Appreciate Functional Coverage.	L3, L4

VII Semester

COMPUTER GRAPHICS AND IMAGE PROCESSING			
Course Code	BUE703	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	04	Exam Hours	03
Course Learning Objectives: This course will enable students to: CLO 1. Overview of Computer Graphics along with its applications. CLO 2. Exploring 2D and 3D graphics mathematics along with OpenGL API's. CLO 3. Use of Computer graphics principles for animation and design of GUI's . CLO 4. Introduction to Image processing and Open CV. CLO 5. Image segmentation using Open CV.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it. 6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Overview: Computer Graphics hardware and software and OpenGL: Computer Graphics: Video Display Devices, Raster-Scan Systems Basics of computer graphics, Application of Computer Graphics. OpenGL: Introduction to OpenGL, coordinate reference frames, specifying two-dimensional world coordinate reference frames in OpenGL, OpenGL point functions, OpenGL line functions, point attributes, line attributes, curve attributes, OpenGL point attribute functions, OpenGL line attribute functions, Line drawing algorithms (DDA, Bresenham's). RBT Levels: L1, L2			
Module-2			
2D and 3D graphics with OpenGL: 2D Geometric Transformations: Basic 2D Geometric Transformations, matrix representations and homogeneous coordinates, 2D Composite transformations, other 2D transformations, raster methods for geometric transformations, OpenGL raster transformations, OpenGL geometric transformations function, 3D Geometric Transformations: Translation, rotation, scaling, composite 3D transformations, other 3D transformations, OpenGL geometric transformations functions. 3D Geometric Transformations: Translation, rotation, scaling, composite 3D transformations, other 3D transformations, OpenGL geometric transformations functions. RBT Levels: L1, L2			
Module-3			
Interactive Input Methods and Graphical User Interfaces: Graphical Input Data, Logical Classification of Input Devices, Input Functions for Graphical Data , Interactive Picture-Construction Techniques, Virtual-Reality Environments, OpenGL Interactive Input-Device Functions, OpenGL Menu Functions , Designing a Graphical User Interface. Computer Animation: Design of Animation Sequences, Traditional Animation Techniques, General Computer-Animation Functions, Computer-Animation Languages, Character Animation, Periodic Motions, OpenGL Animation Procedures. RBT Levels: L1, L2			
Module-4			
Introduction to Image processing: overview, Nature of IP, IP and its related fields, Digital Image representation, types of images. Digital Image Processing Operations: Basic relationships and distance metrics, Classification of Image processing Operations. RBT Levels: L2, L3			

Module-5
Image Segmentation: Introduction, classification, detection of discontinuities, Edge detection (up to canny edge detection (included), Thresholding, Region-Based Segmentation. RBT Levels: L2, L3
Course Outcomes: At the end of the course the student will be able to: • CO 1. Construct geometric objects using Computer Graphics principles and OpenGL APIs. • CO 2. Use OpenGL APIs and related mathematics for 2D and 3D geometric Operations on the objects. • CO 3. Design GUI with necessary techniques required to animate the created objects • CO 4. Apply OpenCV for developing Image processing applications. • CO5. Apply Image segmentation techniques along with programming, using OpenCV.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: • There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. • Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks • Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) • The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). 1. The question paper will have ten questions. Each question is set for 20 marks. 2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. 3. The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.
Suggested Learning Resources: Textbooks 1. Donald D Hearn, M Pauline Baker and Warren Carithers: Computer Graphics with OpenGL 4th Edition, Pearson, 2014 2. S. Sridhar, Digital Image Processing, second edition, Oxford University press 2016. Reference Books 1. Edward Angel: Interactive Computer Graphics- A Top Down approach with OpenGL, 5th edition. Pearson Education, 2008. 2. James D Foley, Andries Van Dam, Steven K Feiner, John F Huges Computer graphics with OpenGL: Pearson education.

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/

Low Power VLSI Design		Semester	VII
Course Code	BUE714A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - To study State-of-the art approaches of power estimation and reduction. - To understand power dissipation at various levels of design - To measure the performance of power dissipation in various Circuits.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Chalk and Talk - PowerPoint Presentation and Videos - Flipped Classes - Practice session			
Module-1			
Introduction: Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits Simulation Power Analysis: SPICE Basics, SPICE Power Analysis RBT Level: L1, L2			
Module-2			
Simulation Power Analysis: Discrete Transistor Modeling and Analysis, Gate-level Logic Simulation, Architecture-level Analysis, Data Correlation analysis in DSP system Probabilistic Power Analysis: Random Logic Signals, Probabilistic Power Analysis Techniques, Signal Entropy RBT Level: L1, L2			
Module-3			
Circuit: Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special Latches and Flip-flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage RBT Level: L1, L2			
Module-4			
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. Special Techniques: Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques. RBT Level: L2, I3			
Module-5			
Special Techniques :CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Wordline and Reduced Bitline Swing Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers: Clock driving schemes, Buffer Insertion in clock tree, Zero skew vs Tolerable skew: Derivation of Tolerable skew, A two level clock distribution scheme, Chip package Co-design of clock network. RBT Level: L2, L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation-based approaches and probabilistic analysis
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Use special power reduction techniques in SRAM memory cell.
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

TEXTBOOKS

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998
2. Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.

REFERENCE BOOK(s):

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic, 1995.
3. A Bellamour and M I Elmasri, "Low power VLSI CMOS circuit design", Kluwer Academic, 1995.

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/courses
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
• Quiz • Seminars

RISK -V Processor		Semester	VII
Course Code	BUE714B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: This course will enable students to: - To understand various operands instructions of RISK-V Processor. - To know the RISK-V Processor architecture. - To understand the register architecture and addressing modes. - Analyse the difference between Arrays and Pointers. - To learn about the RISK-V architecture, instruction set, and ecosystem.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Chalk and Talk. - Power Presentation and Videos. - Flipped Classes. - Practice Sessions.			
Module-1 Instructions Language of the Computer: Introduction , Operations of the Computer: Hardware, Operands of the Computer Hardware: Memory Operands, Constant or Immediate Operands, Signed and Unsigned Numbers. RBT Level: L1,L2			
Module-2 Representing Instructions in the Computer: RISC-V Fields, Logical Operations, Instructions for Making Decisions: Loops, Bounds Check Shortcut, Case/Switch Statement, Supporting Procedures in Computer Hardware: Using More Registers, Nested Procedures, Allocating Space for New Data on the Stack. RBT Level: L1,L2			
Module-3 Allocating Space for New Data on the Heap: Communicating with People, Characters and Strings in Java, RISC-V Addressing for Wide Immediates and Addresses: Wide Immediate Operands, Addressing in Branches, Decoding Machine Language, Parallelism and Instructions: Synchronization, Translating and Starting a Program, Compiler, Assembler, Linker. RBT Levels: L1,L2			
Module-4 Parallelism and Instructions: Loader , Dynamically Linked Libraries, Starting a Java Program, A C Sort Example to Put it All Together: The Procedure swap, The Procedure sort , Arrays versus Pointers: Array Version of Clear, Pointer Version of Clear, Comparing the Two Versions of Clear, Advanced Material: Compiling C and Interpreting Java, Advanced Material: Compiling C and Interpreting Java: Compiling C, The Front End, High-Level Optimizations. RBT Levels: L2,L3			
Module-5 Local and Global Optimizations: Register Allocation, Code Generation, Interpreting Java, Interpretation, Compiling for Java, Invoking Methods in Java, A Sort Example in Java, MIPS Instructions. RBT Levels: L2,L3			

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

CO1: Understand the basic hardware of computers and their different operations.

CO2: Describe the different fields of RISK V processor and instructions.

CO3: Apply and use Programming Techniques for different End Uses

CO4: Describe the code design process Java and C interpretation.

CO5: Understand the local and global optimization from high level uses.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:**Books**

1. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
2. "CMOS Digital Integrated Circuits Analysis and Design"-Sung-Mo Kang, Yusuf Leblebici, 3rd Edition.

Web links and Video Lectures (e-Resources):

- nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz
- Seminar
- Assignments

CLOUD COMPUTING		Semester	VII
Course Code	BUE714C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: • Introduce the rationale behind the cloud computing revolution and the business drivers. • Introduce various models of cloud computing • Introduction on how to design cloud native applications, the necessary tools and the design tradeoffs. • Realize the importance of Cloud Virtualization, Abstraction`s and Enabling Technologies and cloud security.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. 2. Show Video/animation films to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students` Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. 6. Topics will be introduced in a multiple representation. 7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Introduction: Introduction ,Cloud Computing at a Glance, Historical Developments, Building Cloud Computing Environments, Amazon Web Services (AWS), Google AppEngine, Microsoft Azure, Hadoop, Force.com and Salesforce.com, Manjrasoft Aneka.			
RBT Levels: L1, L2			
Module-2			
Virtualization: Introduction, Characteristics of Virtualized, Environments Taxonomy of Virtualization Techniques, Execution Virtualization, Other Types of Virtualization, Virtualization and Cloud Computing, Pros and Cons of Virtualization, Technology Examples.			
RBT Levels: L2			
Module-3			
Cloud Computing Architecture: Introduction, Cloud Reference Model, Types of Clouds, Economics of the Cloud, Open Challenges.			
RBT Levels: L2			
Module-4			
Cloud Security: Risks, Top concern for cloud users, privacy impact assessment, trust, OS security, VM Security, Security Risks posed by shared images and management OS.			
RBT Levels: L2			
Module-5			
Cloud Platforms in Industry Amazon web services: Compute services, Storage services, Communication services, Additional services. Google AppEngine: - Architecture and core concepts, Application life cycle, Cost model, Observations.			
Cloud Applications: Scientific applications: - HealthCare: ECG analysis in the cloud, Biology: gene expression			

data analysis for cancer diagnosis, Geoscience: satellite image processing. Business and consumer applications: CRM and ERP, Social networking, media applications.

RBT Levels: L2, L3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

- CO 1. Understand and analyze various cloud computing platforms and service provider.
- CO 2. Illustrate various virtualization concepts.
- CO 3. Identify the architecture, infrastructure and delivery models of cloud computing.
- CO 4. Understand the Security aspects of CLOUD.
- CO 5. Define platforms for development of cloud applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbooks:

1. Rajkumar Buyya, Christian Vecchiola, and Thamrai Selvi Mastering Cloud Computing McGraw Hill Education.
2. Dan C. Marinescu, Cloud Computing Theory and Practice, Morgan Kaufmann, Elsevier 2013.

Reference Books:

1. Toby Velte, Anthony Velte, Cloud Computing: A Practical Approach, McGraw-Hill Osborne Media.
2. George Reese, Cloud Application Architectures: Building Applications and Infrastructure in the Cloud, O'Reilly Publication.
3. John Rhoton, Cloud Computing Explained: Implementation Handbook for Enterprises, Recursive Press.

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Seminar • Quiz • Group Discussion

BIG DATA ANALYTICS		Semester	VII
Course Code	BUE714D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course objectives: - Understand fundamentals and applications of Big Data analytics - Explore the Hadoop framework and Hadoop Distributed File system and essential Hadoop Tools. - Illustrate the concepts of NoSQL using MongoDB and Cassandra for Big Data. - Employ MapReduce programming model to process the big data. - Understand various machine learning algorithms for Big Data Analytics, Web Mining and Social Network Analysis.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. - Show Video/animation films to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. - Topics will be introduced in a multiple representation. - Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. - Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Introduction to Big Data Analytics: Big Data, Scalability and Parallel Processing, Designing Data Architecture, Data Sources, Quality, Pre-Processing and Storing, Data Storage and Analysis, Big Data Analytics Applications and Case Studies.			
RBT Levels: L1, L2			
Module-2			
Introduction to Hadoop: Introduction, Hadoop and its Ecosystem, Hadoop Distributed File System, MapReduce Framework and Programming Model, Hadoop Yarn, Hadoop Ecosystem Tools.			
Hadoop Distributed File System Basics: HDFS Design Features, Components, HDFS User Commands.			
Essential Hadoop Tools: Using Apache Pig, Hive, Sqoop, Flume, Oozie, HBase.			
RBT Levels: L2			
Module-3			
NoSQL Big Data Management, MongoDB and Cassandra:: Introduction, NoSQL Data Store, NoSQL Data Architecture Patterns, NoSQL to Manage Big Data, Shared-Nothing Architecture for Big Data Tasks, MongoDB, Databases, Cassandra Databases.			
RBT Levels: L2			
Module-4			
Introduction to MapReduce: Introduction, MapReduce Map Tasks, Reduce Tasks and MapReduce Execution, Composing MapReduce for Calculations and Algorithms, Hive, HiveQL, Pig.			
RBT Levels: L2			

Module-5
Machine Learning Algorithms for Big Data Analytics: Introduction, Estimating the relationships, Outliers, Variances, Probability Distributions, and Correlations, Regression analysis, Finding Similar Items, Similarity of Sets and Collaborative Filtering, Frequent Itemsets and Association Rule Mining. Text, Web Content, Link, and Social Network Analytics: Introduction, Text mining, Web Mining, Web Content and Web Usage Analytics, Page Rank, Structure of Web and analyzing a Web Graph, Social Network as Graphs and Social Network Analytics. RBT Levels: L2, L3
Course outcome (Course Skill Set) At the end of the course, the student will be able to : • CO 1. Understand fundamentals and applications of Big Data analytics. • CO 2. Investigate Hadoop framework, Hadoop Distributed File system and essential Hadoop tools. • CO 3. Illustrate the concepts of NoSQL using MongoDB and Cassandra for Big Data. • CO 4. Demonstrate the MapReduce programming model to process the big data along with Hadoop tools. • CO 5. Apply Machine Learning algorithms for real world big data, web contents and Social Networks to provide analytics with relevant visualization tools.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: • There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. • Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks • Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) • The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.
Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). 1. The question paper will have ten questions. Each question is set for 20 marks. 2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. 3. The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.
Suggested Learning Resources: Textbooks: 1. Raj Kamal and Preeti Saxena, "Big Data Analytics Introduction to Hadoop, Spark, and MachineLearning", McGraw Hill Education, 2018 ISBN: 9789353164966, 9353164966

2. Douglas Eadline, "Hadoop 2 Quick-Start Guide: Learn the Essentials of Big Data Computing in the Apache Hadoop 2 Ecosystem", 1 stEdition, Pearson Education, 2016. ISBN13: 978-9332570351. Reference Books: 1. Tom White, "Hadoop: The Definitive Guide", 4 th Edition, O'Reilly Media, 2015.ISBN-13: 978-9352130672 2. Boris Lublinsky, Kevin T Smith, Alexey Yakubovich, "Professional Hadoop Solutions", 1st Edition, Wrox Press, 2014ISBN-13: 978-8126551071. 3. Eric Sammer, "Hadoop Operations: A Guide for Developers and Administrators", 1st Edition, O'Reilly Media, 2012, ISBN-13: 978-9350239261. 4. Arshdeep Bahga, Vijay Madiseti, "Big Data Analytics: A Hands-On Approach", 1st Edition, VPT Publications, 2018. ISBN-13: 978-0996025577 .
Web links and Video Lectures (e-Resources): • https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Seminar • Quiz • Group Discussion

Verilog HDL		Semester	VII
Course Code	BUE755A	CIE Marks	50
Teaching Hours/Week(L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature(SEE)	Theory		
Course objectives: • Learn different Verilog HDL Constructs. • Familiarize the different levels of abstraction in Verilog. • Understand Verilog tasks , functions and directives. • Understand timing and delay simulation. • Understand the concept of logic synthesis and its impact in verification.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. 6. Introduce Topics in manifold representations. 7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world-and when that’s possible, it helps improve the students' understanding.			
Module-1			
Overview of digital design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL? Trends in HDL Hierarchical Modelling Concepts: Top down and bottom-up design methodology, difference between modules and module instances, parts of a simulation, design block, stimulus block. RBT Levels: L1, L2			
Module-2			
Basic Concepts: Lexical conventions, data types, system tasks, compiler directives. Modules and ports: Module definition, port declaration, connecting ports, Hierarchical name referencing. RBT Levels: L1, L2			
Module-3			
Gate level modeling: Modelling using basic Verilog gate primitives, description of and /or and buf/not type gates, rise, fall and turn off delays, min, max and typical delays Data flow modeling: Continuous assignments, delay specification, expressions, operators, operand sand operate types. RBT Levels: L2			

Module-4
Behavioral modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, multi way branching, loops, sequential and parallel blocks. Tasks and functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. RBT Levels: L2, L3
Module-5
Useful Modeling techniques: Procedural continuous assignments, over riding parameters, conditional compilation, and execution, useful system tasks Logic Synthesis with Verilog: Logic synthesis, impact of logic synthesis, Verilog HDL synthesis, synthesis design flow, verification of gate level net list. RBT Levels: L2, L3
Course outcome(Course Skill Set) At the end of the course, the student will be able to: • Write Verilog program singate, dataflow(RTL), behavioral and switch modeling levels of abstraction. • Design and verify the functionality of digital circuit and system, using test benches • Identify the suitable abstraction level for a particular digital system. • Write the programs more effectively using Verilog tasks, function sand directives. • Program timing and delay simulation and interpret the various constructs in logic synthesis.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: • There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. • Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks • Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) • The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). 1. The question paper will have ten questions. Each question is set for 20 marks. 2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. 3. The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:**Books**

1. Samir Palnitkar, "Verilog HDL: A guide to digital design and synthesis", Pearson Education, II Edition.

Reference Books:

1. Donald E Thomas, Philip R Moorby, "The Verilog hardware description Language",
2. Springer Science Business Media, LLC, 5th Edition
3. Michael D Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI), II Edition.
4. Padmanabhan, Tripura Sunadri, "Design through Verilog HDL", Wiley, 2016.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/courses/>

Activity Based Learning (Suggested Activities in Class)/Practical Based learning

- VHDL based projects for different applications
- Seminars
- Quizzes
- Assignments

COMPUTER ORGANIZATION			
Course Code	BUE755B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	3 Hours/week	Total Marks	100
Credits	03	Exam Hours	03
Course Objectives: • CL01.Understanding of Computer Architecture: Gain foundational knowledge of the key components of computer systems, including CPUs, memory, storage, and input/output systems. • CL02.Understand the concepts of instruction sets, addressing modes, and how they influence software design and hardware implementation. • CL03.Explore the organization of memory systems, including cache memory, virtual memory, and storage hierarchies. • CL04.Develop skills in writing and understanding assembly language to bridge the gap between high-level programming and hardware. • CL05.Examine concepts of parallelism and distributed systems, including multi-core processors • CL06.Apply theoretical concepts to real-world scenarios, fostering problem-solving skills through projects and practical exercises.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. 6. Introduce Topics in manifold representations. 7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.			
RBT Levels: L1,L2			
Module-2			
Input/output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices. Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.			
RBT Levels:L1,L2			
Module-3			
Basic Processing Unit: Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction. Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.			
RBT Levels:L1,L2			
Module-4			
Embedded Systems: Examples of embedded Systems, Microwave Oven, Digital Camera, Home Telemetry, Processor Chips for Embedded Applications.			

Embedded Processor Families: Microcontroller Based on the Intel 8051, Motorola Microcontrollers, ARM Microcontrollers.
RBT Levels: L2,L3
Module-5
Large Computer Systems: Forms of Parallel Processing, Array Processors, The Structure of General-Purpose Multiprocessors. Memory Organization in Multiprocessors. Multicomputers: Local Area Networks, Ethernet(CSMA/CD) BUS, Token Ring, Network of Workstations
RBT Levels: L2,L3
Course Outcomes (Course Skill Set): At the end of the course the student will be able to: CO1: Describe the fundamentals of machine instructions, addressing modes and Processor performance. CO2: Explain the approaches involved in achieving communication between processor and I/O devices. CO3: Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance. CO4: Understand the working of Embedded systems and its processor Families. CO5: Design analysis of Large Computer systems and Multicomputers.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.
Continuous Internal Evaluation: - There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. - Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks - Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) - The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.
Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.
Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). - The question paper will have ten questions. Each question is set for 20 marks. - There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. - The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.
Textbooks: Carl Hamcher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill.
Weblinks and Video Lectures (e-Resources):

• nptel.ac.in

ARM MICROCONTROLLER		Semester	VII
Course Code	BUE755C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	Theory		
Course Objectives: - Understand the fundamentals of ARM-based systems. - Understand ARM programming modules with registers and the CPSR. - Use the various instructions to program the ARM controller. - Program various embedded components using the embedded C program. - Understand the various optimized primitives used in ARM assembly code.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. - Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. - Show Video/animation films to explain functioning of various concepts. - Encourage collaborative (Group Learning) Learning in the class. - Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. - Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it. - Topics will be introduced in a multiple representation. - Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. - Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
ARM Embedded Systems: The RISC design philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts, and the Vector Table, Core Extensions. RBT Levels: L1, L2			
Module-2			
Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Software Interrupt Instructions, Program Status Register Instructions, Coprocessor Instructions, Loading Constants, ARMv5E Extensions, Conditional Execution. RBT Levels: L2			
Module-3			
C Compilers and Optimization: :Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Pointer Aliasing, Structure Arrangement, Bit-fields, Unaligned Data and Endianness, Division, Floating Point, Inline Functions and Inline Assembly, Portability Issues. RBT Levels: L2, L3			
Module-4			
ARM programming using Assembly Language: Writing Assembly code, Profiling and cycle counting, instruction scheduling, Register Allocation, Conditional Execution, Looping Constructs, Bit Manipulation, Efficient Switches, Handling Unaligned Data. RBT Levels: L2, L3			

Module-5
Optimized Primitives: Double-Precision, Integer Multiplication, Integer Normalization and Count Leading Zeros, Division, Square Roots, Transcendental Functions: log, exp, sin, cos. RBT Levels: L2, L3
Course outcome (Course Skill Set) At the end of the course, the student will be able to : - CO 1. Describe the ARM microcontroller's architectural features and program module. - CO 2. Apply the knowledge gained from programming on ARM to different applications. - CO 3. Explain C-Compilers and optimization.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: - There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. - Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks - Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) - The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). - The question paper will have ten questions. Each question is set for 20 marks. - There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. - The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.
Suggested Learning Resources: Textbooks: - Andrew N Sloss, Dominic Symes and Chris Wright, ARM system developers guide, Elsevier, Morgan Kaufman publishers, 2008. Reference Books: - RaghuNandan. G.H, Microcontroller (ARM) and Embedded System, Cengage learning Publication, 2019. - The Insider's Guide to the ARM7 Based Microcontrollers, Hitex Ltd., 1st edition, 2005. - Steve Furber, ARM System-on-Chip Architecture, Second Edition, Pearson, 2015.
Web links and Video Lectures (e-Resources): https://nptel.ac.in/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Seminar
- Quiz
- Group Discussion

OPERATIONAL AMPLIFIER			
Course Code	BUE755D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	3 Hours/week	Total Marks	100
Credits	03	Exam Hours	03
Course Objectives: • CLO1. Define and describe various parameters of Op-Amp, its characteristics and Specifications. • CLO2. Discuss the effects of Input and Output voltage range upon Op-Amp circuits. • CLO3. Sketch and Analyze Op-Amp circuits to determine Input Impedances, output Impedances and other performance parameters. • CLO4. Sketch and Explain typical Frequency Response graphs for each of the Filter circuits. Showing Butterworth and Chebyshev responses where ever appropriate. • CLO4. Describe and Sketch the various switching circuits of Op-Amps and analyze its operations. • CLO6. Differentiate between various types of DACs and ADCs and evaluate the performance of each with neat circuit diagrams and assuming suitable inputs.			
Teaching-Learning Process (General Instructions) These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. 1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes. 2. Use of Video/Animation to explain functioning of various concepts. 3. Encourage collaborative (Group Learning) Learning in the class. 4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking. 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it. 6. Introduce Topics in manifold representations. 7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.			
Module-1			
Operational Amplifier Fundamentals: Basic Op-amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations. OP-Amps as DC Amplifiers – Biasing OP-amps, Direct coupled voltage followers, Non-inverting amplifiers, inverting amplifiers, Summing amplifiers, and Difference amplifiers. Interpretation of OP-amp LM741 & TL081 datasheet. RBT Levels: L1, L2			
Module-2			
Op-Amps as AC Amplifiers: Capacitor coupled voltage follower, High input impedance– Capacitor coupled voltage follower, Capacitor coupled non inverting amplifiers, High input impedance – Capacitor coupled Non inverting amplifiers, Capacitor coupled inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled difference amplifier. OP-Amp Applications: Voltage sources, current sources and current sinks, current amplifiers, instrumentation amplifier, precision rectifiers. RBT Levels: L1, L2			
Module-3			
More Applications: Limiting circuits, Clamping circuits, Peak detectors, Sample and hold circuits, V to I and I to V converters, Differentiating Circuit, Integrator Circuit, Phase shift oscillator, Wien bridge oscillator, Crossing detectors, inverting Schmitt trigger. Log and antilog amplifiers, Multiplier and divider. RBT Levels: L2, L3			
Module-4			
Active Filters: First order and second order active Low-pass and high pass filters, Bandpass Filter, Bandstop Filter.			

Voltage Regulators: Introduction, Series Op-amp regulator, IC voltage regulators. 723 general purpose regulators. RBT Levels: L2,L3
Module-5
Phase locked loop: Basic Principles, Phase detector/comparator, VCO. DAC and ADC convertor: DAC using R-2R, ADC using Successive approximation. Other IC Application: 555 timer, Basic timer circuit, 555 timer used as astable and monostable multivibrator. RBT Levels: L2,L3
Course Outcomes (Course Skill Set): At the end of the course the student will be able to: CO1. Explain Op-Amp circuit and parameters including CMRR, PSRR, Input & Output Impedances and Slew Rate. CO2. Design Op-Amp based Inverting, Non-inverting, Summing & Difference Amplifier, and AC Amplifiers including Voltage Follower. CO3. Test circuits of Op-Amp based Voltage/ Current Sources & Sinks, Current, Instrumentation and Precision Amplifiers. CO4. Test circuits of Op-Amp based linear and non-linear circuits comprising of limiting, clamping, Sample & Hold, Differentiator/ Integrator Circuits, Peak Detectors, Oscillators and Multiplier & Divider. CO5. Design first & second order Low Pass, High Pass, Band Pass, Band Stop Filters and Voltage Regulators using Op-Amps. CO6. Explain applications of linear ICs in phase detector, VCO, DAC, ADC and Timer.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.
Continuous Internal Evaluation: - There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component. - Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks - Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) - The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.
Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.
Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours). - The question paper will have ten questions. Each question is set for 20 marks. - There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. - The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.

Textbooks

1. Operational Amplifiers and Linear IC's||, David A. Bell, 2nd edition, PHI/Pearson, 2004. ISBN 978-81-203-2359-9.
2. Linear Integrated Circuits||, D. Roy Choudhury and Shail B. Jain, 4th edition, Reprint 2006, New Age International ISBN 978-81-224-3098-1.

Reference Books

1. Ramakant A Gayakwad, "Op-Amps and Linear Integrated Circuits", Pearson, 4th Ed, 2015. ISBN 81-7808-501-1.
2. B Somanathan Nair, "Linear Integrated Circuits: Analysis, Design & Applications", Wiley India, 1st Edition, 2015.
3. James Cox, "Linear Electronics Circuits and Devices", Cengage Learning, Indian Edition, 2008, ISBN-13: 978-07-668-3018-7

Weblinks and Video Lectures (e-Resources):

- <https://nptel.ac.in/>