

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING SECOND INTERNAL SCHEME

SUB: DIGITAL DESIGN AND COMPUTER ORGANIZATION

SUB CODE: BCS302

FACULTY NAME: PROF. AKSHATHA S.A

MAX. MARKS: 50

DATE: 25/12/2024

Answer Any One Full Question from each part

		PART A	MARKS SPLIT UP	M	СО	BTL
	a)	Design a BCD-to-excess-3 code converter Explaining the steps Truth Table Kmap Result	2 3 4 1	10	COA	L3
	b)	Design and explain four bit subtractor. Illustrate how overflow can be identified in subtractor. Diagram Explanation about Subtractor Explanation about overflow	3 4 3	10	СОД	L2
	c)	Explain the concept of multiplexer. Diagram Explanation	4 6	10	CO4	L2'
2.	a)	What is latch? With a neat diagram, explain S-R latch using NOR gate. Definition Truth Table Diagram Explanation	2 2 3 3	10	CO4	. L3
	b)	What is priority encoder? Design 4:2 priority encoder with necessary diagram. Definition	3 3 4	10	COA	L

		Design and explain four bit adder with carry look ahead.	3 4	10	СОД	L3
	c)	Circuit Diagram				
		Explanation about adder				
		Explanation about carry look ahead	3			
		PART B				
	a)	With neat sketches, explain various methods for		10	COL	L3
3	3	handling multiple interrupt requests raised by multiple devices.				
	1.6	Explain how interrupt occurs	2			
		Explain Vector interrupt method	2			
	132	Explain priority method	3			
	10	Explain Daisy chain method	3			
	b)	What is DMA Bus arbitration? Explain different bus arbitration Techniques.		10	COL	L3
		Diagram of DMA bus arbitration	3			
		Explain 4 types of bus arbitration technique	7			
		OR				
	a)	Draw a neat block diagram of memory hierarchy in a computer system. Discuss the variation of size, speed	Mark	10	COL	L3
		and cost per bit in the hierarchy.				
		block diagram	3	1		
		variation of size, speed and cost per bit in the hierarchy	7			
	b)	Discuss different types of mapping function of caches.		10	COL	L3
		Explain 4 methods each of 2.5 marks	2.5*4			

Course Coordinator

Module Coordinator

HOD