Bearys Institute of Technology
MANGALORE

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
SECOND INTERNAL ASSESSMENT TEST

SUB: DIGITAL DESIGN AND COMPUTER ORGANIZATION

SUB CODE: BCS302 **MAX. MARKS: 50**

FACULTY NAME: PROF. AKSHATHA S.A **DATE: 25/12/2024**

*Answer **Any One Full Question** from each part*

		PART A	M	CO	BTL
1.	a)	Design a BCD-to-excess-3 code converter	10	CO4	L3
	b)	Design and explain four bit subtractor. Illustrate how overflow can be identified in subtractor.	10	CO4	L2
	c)	Explain the concept of multiplexer.	10	CO4	L2
		OR			
2.	a)	What is latch? With a neat diagram, explain S-R latch using NOR gate.	10	CO4	L3
	b)	What is priority encoder? Design 4:2 priority encoder with necessary diagram.	10	CO4	L2
	c)	Design and explain four bit adder with carry look ahead.	10	CO4	L3
		PART B			
3	a)	With neat sketches, explain various methods for handling multiple interrupt requests raised by multiple devices.	10	CO2	L3
	b)	What is DMA Bus arbitration? Explain different bus arbitration Techniques.	10	CO2	L3
		OR			
4	a)	Draw a neat block diagram of memory hierarchy in a computer system. Discuss the variation of size, speed and cost per bit in the hierarchy.	10	CO2	L3
	b)	Discuss different types of mapping function of caches.	10	CO2	L3

Course Coordinator

Module Coordinator

HOD