COURSE BOOK

Duration of Semester	19 Aug 2024 To 21 Dec 2024	**# of Lecture Hours/ Week**	3
Degree	BE	**Dept-Sem-Sec**	CS-3-A
Course Name	DIGITAL DESIGN & COMPUTER ORGANIZATION	**Course Code**	BCS302
IA Marks	50	**Exam Marks**	50
Exam Hours	3	**Credits**	4
Name of the Faculty	Ms Akshatha S A	**# of Lecture Hours**	50

Time Slot

Mon	12:15 PM - 01:05 PM	**Thu**	-
Tue	10:15 AM - 11:05 AM	**Fri**	09:20 AM - 10:15 AM
Wed	-	**Sat**	11:20 AM - 12:15 PM

Lesson Plan And Execution

Source Material List

TEXT 1	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.
TEXT 2	Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5th Edition, Tata McGraw Hill.

Course Objective List

1	To demonstrate the functionalities of binary logic system
2	To explain the working of combinational and sequential logic system
3	To realize the basic structure of computer system
4	To illustrate the working of I/O operations and processing unit

Course Outcome List

1	Apply the K–Map techniques to simplify various Boolean expressions.
2	Design different types of combinational and sequential circuits along with Verilog programs.
3	Describe the fundamentals of machine instructions, addressing modes and Processor performance.
4	Explain the approaches involved in achieving communication between processor and I/O devices.
5	Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance.

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
Module 1									
1	P	19 Aug 2024	Binary Logic			0 hour: 50 min		Lecture	
1	E	20 Aug 2024	Binary Logic	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 50 min	UNDERSTAND	Lecture	
2	P	20 Aug 2024	Basic Theorems And Properties Of Boolean Algebra			0 hour: 50 min		Lecture	
2	E	21 Aug 2024	Basic Theorems And Properties Of Boolean Algebra	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 50 min	REMEMBER	Lecture	
3	P	23 Aug 2024	Boolean Functions			0 hour: 55 min		Lecture	
3	E	22 Aug 2024	Boolean Functions	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e,	CO 1	0 hour: 55 min	UNDERSTAND	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				Pearson Education.					
4	P	24 Aug 2024	Digital Logic Gates			0 hour: 55 min		Lecture	
4	E	23 Aug 2024	Digital Logic Gates	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 55 min	UNDERSTAND	Lecture	
5	P	26 Aug 2024	Introduction			0 hour: 50 min		Lecture	
5	E	23 Aug 2024	Introduction	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 50 min	REMEMBER	Lecture	
6	P	27 Aug 2024	The Map Method			0 hour: 50 min		Lecture	
6	E	24 Aug 2024	The Map Method	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design,	CO 1	0 hour: 50 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				5e, Pearson Education.					
7	P	30 Aug 2024	Four-Variable Map			0 hour: 55 min		Lecture	
7	E	24 Aug 2024	Four-Variable Map	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 55 min	UNDERSTAND	Lecture	
8	P	31 Aug 2024	Don't-Care Conditions			0 hour: 55 min		Lecture	
8	E	29 Aug 2024	Don't-Care Conditions	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 55 min	REMEMBER	Lecture	
9	P	2 Sep 2024	NAND and NOR Implementation			0 hour: 50 min		Lecture	
9	E	29 Aug 2024	NAND and NOR Implementation	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design,	CO 1	0 hour: 50 min	UNDERSTAND	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				5e, Pearson Education.					
10	P	3 Sep 2024	Other Hardware Description Language – Verilog Model of a simple circuit			0 hour: 50 min		Lecture	
10	E	2 Sep 2024	Other Hardware Description Language – Verilog Model of a simple circuit	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 1	0 hour: 50 min	UNDERSTAND	Lecture	
Module 2									
11	P	6 Sep 2024	Introduction, Combinational Circuits			0 hour: 55 min		Lecture	
20	E	23 Sep 2024	Flip-Flops	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	REMEMBER	Lecture	
12	P	7 Sep 2024	Design Procedure, Binary Adder-Subtractor			0 hour: 55 min		Lecture	
25	E	1 Oct 2024	Performance Measurement	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog	CO 2	0 hour: 50 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				Design, 5e, Pearson Education.					
13	P	9 Sep 2024	Decoders, Encoders			0 hour: 50 min		Lecture	
26	E	4 Oct 2024	Memory Location and Addresses	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 50 min	REMEMBER	Lecture	
14	P	10 Sep 2024	Multiplexers,HDL Models of Combinational Circuits – Adder			0 hour: 50 min		Lecture	
27	E	7 Oct 2024	Memory Location and Addresses	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 55 min	REMEMBER	Lecture	
15	P	13 Sep 2024	Multiplexer, Encoder			0 hour: 55 min		Lecture	
28	E	8 Oct 2024	Memory Operations	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog	CO 2	0 hour: 55 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				Design, 5e, Pearson Education.					
16	P	14 Sep 2024	Introduction			0 hour: 55 min		Lecture	
29	E	15 Oct 2024	Instruction and Instruction sequencing	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 50 min	REMEMBER	Lecture	
17	P	16 Sep 2024	Introduction			0 hour: 50 min		Lecture	
32	E	26 Oct 2024	Accessing I/O Devices	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 55 min	UNDERSTAND	Lecture	
18	P	17 Sep 2024	Sequential Circuits			0 hour: 50 min		Lecture	
34	E	4 Nov 2024	Interrupts – Interrupt Hardware	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction	CO 2	0 hour: 50 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				to Verilog Design, 5e, Pearson Education.					
19	P	20 Sep 2024	Storage Elements: Latches			0 hour: 55 min		Lecture	
35	E	5 Nov 2024	Enabling and Disabling Interrupts	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 55 min	UNDERSTAND	Lecture	
20	P	21 Sep 2024	Flip-Flops			0 hour: 55 min		Lecture	
36	E	11 Nov 2024	Handling Multiple Devices	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 55 min	UNDERSTAND	Lecture	
37	E	15 Nov 2024	Direct Memory Access: Bus Arbitration	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design,	CO 2	0 hour: 50 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				5e, Pearson Education.					
Module 3									
21	P	23 Sep 2024	Functional Units, Basic Operational Concepts			0 hour: 50 min		Lecture	
11	E	2 Sep 2024	Introduction, Combinational Circuits	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 55 min	REMEMBER	Lecture	
22	P	24 Sep 2024	Bus structure, Performance – Processor Clock			0 hour: 50 min		Lecture	
12	E	3 Sep 2024	Design Procedure, Binary Adder-Subtractor	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	UNDERSTAND	Lecture	
23	P	27 Sep 2024	Basic Performance Equation			0 hour: 55 min		Lecture	
13	E	6 Sep 2024	Decoders, Encoders	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata	CO 3	0 hour: 50 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				McGraw Hill.					
24	P	28 Sep 2024	Clock Rate			0 hour: 55 min		Lecture	
14	E	9 Sep 2024	Multiplexers, HDL Models of Combinational Circuits – Adder	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata . McGraw Hill.	CO 3	0 hour: 50 min	UNDERSTAND	Lecture	
25	P	30 Sep 2024	Performance Measurement			0 hour: 50 min		Lecture	
15	E	10 Sep 2024	Multiplexer, Encoder	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	UNDERSTAND	Lecture	
26	P	1 Oct 2024	Memory Location and Addresses			0 hour: 50 min		Lecture	
16	E	13 Sep 2024	Introduction	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	UNDERSTAND	Lecture	
27	P	4 Oct 2024	Memory Location and Addresses			0 hour: 55 min		Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
17	E	14 Sep 2024	Introduction	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 50 min	UNDERSTAND	Lecture	
28	P	5 Oct 2024	Memory Operations			0 hour: 55 min		Lecture	
18	E	17 Sep 2024	Sequential Circuits	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 50 min	UNDERSTAND	Lecture	
29	P	7 Oct 2024	Instruction and Instruction sequencing			0 hour: 50 min		Lecture	
19	E	20 Sep 2024	Storage Elements: Latches	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	UNDERSTAND	Lecture	
30	P	8 Oct 2024	Addressing Modes			0 hour: 50 min		Lecture	
21	E	24 Sep 2024	Functional Units, Basic Operational Concepts	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th	CO 3	0 hour: 50 min	UNDERSTAND	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				Edition, Tata McGraw Hill.					
22	E	27 Sep 2024	Bus structure, Performance – Processor Clock	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 50 min	REMEMBER	Lecture	
23	E	28 Sep 2024	Basic Performance Equation	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	UNDERSTAND	Lecture	
24	E	30 Sep 2024	Clock Rate	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 3	0 hour: 55 min	REMEMBER	Lecture	
30	E	18 Oct 2024	Addressing Modes	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog	CO 2	0 hour: 50 min	UNDERSTAND	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				Design, 5e, Pearson Education.					
Module 4									
31	P	11 Oct 2024	Accessing I/O Devices			0 hour: 55 min		Lecture	
31	E	25 Oct 2024	Accessing I/O Devices	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 55 min	UNDERSTAND	Lecture	
32	P	12 Oct 2024	Accessing I/O Devices			0 hour: 55 min		Lecture	
33	E	28 Oct 2024	Interrupts – Interrupt Hardware	M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.	CO 2	0 hour: 50 min	UNDERSTAND	Lecture	
33	P	14 Oct 2024	Interrupts – Interrupt Hardware			0 hour: 50 min		Lecture	
34	P	15 Oct 2024	Interrupts – Interrupt Hardware			0 hour: 50 min		Lecture	
35	P	18 Oct 2024	Enabling and Disabling Interrupts			0 hour: 55 min		Lecture	
36	P	19 Oct 2024	Handling Multiple Devices			0 hour: 55 min		Lecture	
37	P	21 Oct 2024	Direct Memory Access: Bus Arbitration			0 hour: 50 min		Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
38	P	22 Oct 2024	Speed			0 hour: 50 min		Lecture	
39	P	25 Oct 2024	size and Cost of memory systems			0 hour: 55 min		Lecture	
40	P	26 Oct 2024	Cache Memories – Mapping Functions			0 hour: 55 min		Lecture	
Module 5									
41	P	28 Oct 2024	Some Fundamental Concepts: Register Transfers			0 hour: 50 min		Lecture	
38	E	19 Oct 2024	Some Fundamental Concepts: Register Transfers, Performing ALU operations	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 50 min	REMEMBER	Lecture	
42	P	29 Oct 2024	Performing ALU operations			0 hour: 50 min		Lecture	
39	E	22 Nov 2024	fetching a word from Memory, Storing a word in memory	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 55 min	UNDERSTAND	Lecture	
43	P	1 Nov 2024	fetching a word from Memory			0 hour: 55 min		Lecture	
40	E	23 Nov 2024	Execution of a Complete Instruction	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata	CO 5	0 hour: 55 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				McGraw Hill.					
44	P	2 Nov 2024	Storing a word in memory			0 hour: 55 min		Lecture	
41	E	25 Nov 2024	Basic concepts	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 50 min	UNDERSTAND	Lecture	
45	P	4 Nov 2024	Execution of a Complete Instruction			0 hour: 50 min		Lecture	
42	E	29 Nov 2024	Basic concepts	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 50 min	UNDERSTAND	Lecture	
46	P	5 Nov 2024	Basic concepts			0 hour: 50 min		Lecture	
43	E	30 Nov 2024	Role of Cache memory	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 55 min	REMEMBER	Lecture	
47	P	8 Nov 2024	Basic concepts			0 hour: 55 min		Lecture	
44	E	2 Dec 2024	Pipeline Performance	Carl Hamacher, ZvonkoVran	CO 5	0 hour: 55 min	REMEMBER	Lecture	

Period	Plan/ Execution	Date	Topic	Source Materials to be Referred	Course Outcomes	Duration	Bloom's Level	Execution Methods	Learning Validation Method
				SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.					
48	P	9 Nov 2024	Role of Cache memory			0 hour: 55 min		Lecture	
45	E	3 Dec 2024	Pipeline Performance	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 50 min	REMEMBER	Lecture	
49	P	11 Nov 2024	Role of Cache memory			0 hour: 50 min		Lecture	
46	E	6 Dec 2024	Pipeline Performance	Carl Hamacher, ZvonkoVran SafwatZaky, Computer Organizatior 5th Edition, Tata McGraw Hill.	CO 5	0 hour: 50 min	APPLY	Lecture	
50	P	12 Nov 2024	Pipeline Performance			0 hour: 50 min		Lecture	
47	E								
48	E								
49	E								
50	E								

Module No.	# of Classes Planned (Till Date)	Planned Effort (Till Date)	# of Classes Executed (Till Date)	Actual Effort (Till Date)	% Coverage
1	10	8hrs 40min	10	8hrs 40min	100.0
2	10	8hrs 50min	11	9hrs 40min	109.43
3	10	8hrs 40min	14	12hrs 15min	141.35
4	10	8hrs 50min	2	1hrs 45min	19.81
5	10	8hrs 40min	9	7hrs 50min	90.38
Faculty in Charge			**HOD's Signature**		
Signature of Principal (Remarks, If Any)					