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ASSIGNMENT BOOK

NAME OF THE STUDENT : AMRUTHA.T.S

SEM / ACADEMIC YEAR : 3rd 2024 BRANCH : C.S.E SECTION : -

UNIVERSITY SEAT NUMBER : 4BP23CS006

SUBJECT : DCO SUBJECT CODE: .....

	DATE	MAX. MARKS	MARKS OBTAINED	TEACHER'S INITIAL	REMARKS
FIRST ASSIGNMENT	16/12/24	10	10	Abhilash S.A	—
SECOND ASSIGNMENT					
THIRD ASSIGNMENT					
AVERAGE ASSIGNMENT MARKS					

ASSIGNMENT MARKS IN WORDS : Ten

Student

Staff

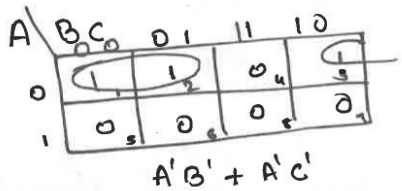
HOD

Design a combination with three input and one output.

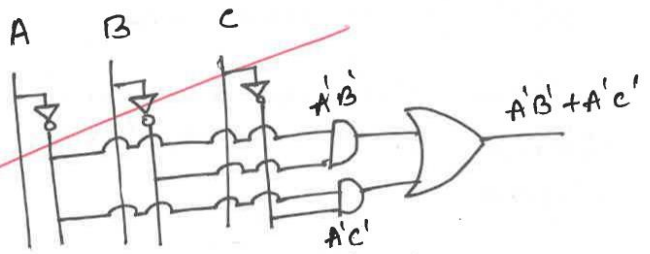
The output is 1 when the binary value of the input is less than or equal to 2. The output is zero otherwise.

The output is 1 when the binary value of the input is an even no.

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

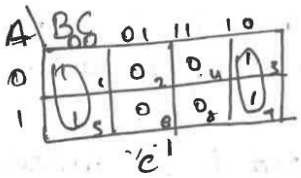


A'B' + A'C'

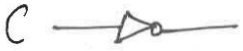


b)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



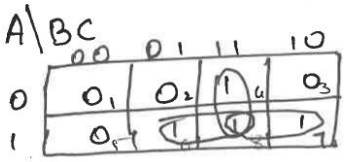
Logic Circuit



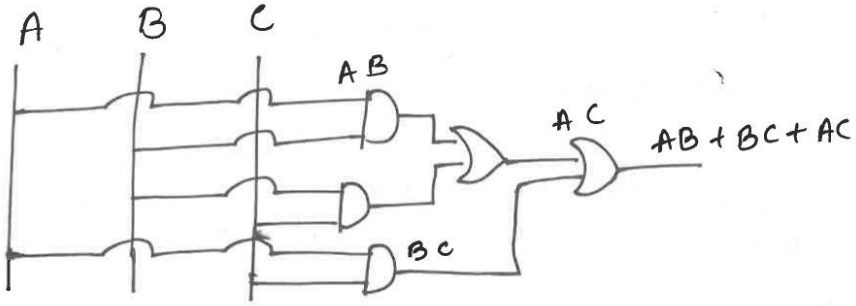
2] A certain combinational circuit use the output 1. If there input variable have more one's then 0 the output is 0 other wise.

Design the above combination circuit by finding the circuits truth table boolean expression and logic diagram.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



$AB + BC + AC$



3] Differentate between latch and flip-flop.

Latches	Flip-flop.
• Latches are said to be level semetic device.	• Flip-flop are edge sensture devices
• Changes as soon as the input changes (while enebeled	• Changes only at the rising or falling edge of the clock signal
• No clock signal.	• Requries a clock signal
• Less stable due to patent late conditions	• More stable as they only change state at specific times
• SR latch, JK latch, D latch	• SR flip-flops, JK filp-flop, J flip-flop, D flip-flop
• Simple storge elements, a sychronous circuit.	• Sequential logic circuits synchoroous system.

4) Obtain a minimum products of sum with a K-map

$F(w,x,y,z) = x'z' + wyz + w'y'z' + x'y$.

$x'z' = wx'yz'$ or $w'x'yz'$

1010 or 0010

$= 10$ $= 2$

$wx'y'z'$ or $w'x'y'z'$

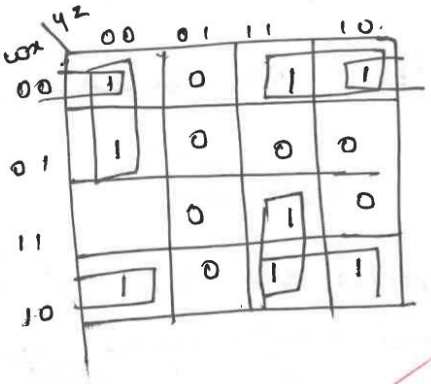
1000 or 0000

$= 8$ $= 0$

$wyz = wxyz$ or $wx'yz'$

1111 or 1010

$= 15$ $= 11$



$w'y'z' = w'xy'z'$ or $w'x'y'z'$

0100 or 0000

$= 4$ $= 0$

$x'y = wx'yz$ or $w'x'yz$ or $wx'yz'$ or $w'x'yz'$

1011 0011 1010 0010

$= 11$ $= 3$ $= 10$ $= 2$

$F(w,x,y,z) = (0,2,3,4,8,10,11,15)$

$= 53$.

5 Find the minimum sum of products for each function using a k-map

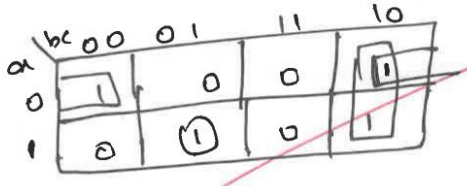
1] $F_1(a,b,c) = M_0 + M_2 + M_5 + M_6$

2] $F_2(d,e,f) = \Sigma m(0,1,2,4)$

3] $F_2(r,s,t) = rt' + r's' + r's$

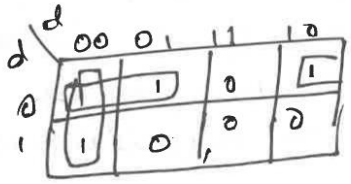
i] $F(a,b,c) = M_0 + M_2 + M_5 + M_6$

$F(a,b,c) = \Sigma m(0,2,5,6)$



$F(a,b,c) = a'c + bc' + ab'c$

ii] $F(d,e,f) = \Sigma m(0,1,2,4)$



$F(d,e,f) = \bar{e}\bar{f} + \bar{d}\bar{e} + \bar{d}\bar{f}$

iii) $F(r,s,t) = rt' + r's' + r's$

$rt' = rst'$ or $rs't'$

100 or 100

$= 6$ $= 4$

$r's' = r's't$ or $r's't'$

001 000

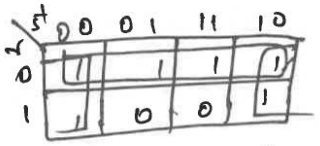
$= 1$ $= 0$

$r's = r'st$ or $r'st'$

011 010

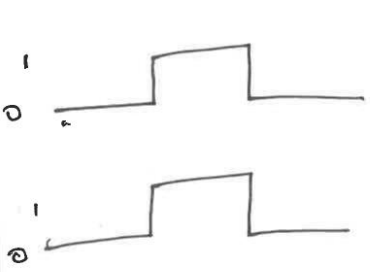
$= 3$ $= 2$

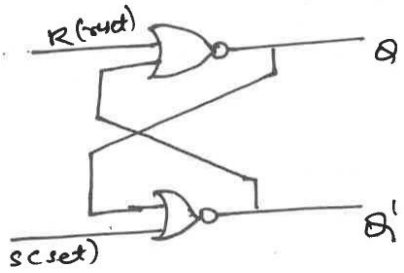
$F(r,s,t) = (0, 1, 2, 3, 4, 6)$



$F(r,s,t) = r' + t'$

5] What is latch with a neat diagram explain SR latch using NOR gate. Derive characteristive equation latches are said to be level sensitive devices Although latches are useful for storing binary information and for the design of synchronous sequential. They are not Pratical for use as storage elements in synchronous sequential circuits.





logic diagram.

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

- The SR, latch is a circuit with two cross coupled NOR gates or two cross-coupled NAND gates, and two inputs labelled S for set, and R for reset.
- The SR latch constructed with two cross coupled NOR gates
- The latch has two useful states.
- Output Q and Q' are normally the complement of each other
- However the both inputs are equal to 1 at the same time, a condition in which both outputs are equal to 0 (rather than be mutually complimentry) occurs.
- If both inputs are then switched to simultanously the device will enter an unpredictable as undefined state, called a mutable state.
- Consequently in pratical applications, setting both inputs to 1 is for biddem.

Characteristic equations:-

The logical properties of a flip-flop as described in the characteristic table, can be expressed algebrically with a characteristic equation for the D flip-flop we have the characteristic equation

$$Q(t+1) = D$$

which states that the next state of the output will be equal to the value of input D, in the present state. The characteristic equation for the JK flip-flop can be derived from the table characteristic table we obtain $Q(t+1) = JQ' + K'Q$

where Q is the value of the flip-flop output prior to the application of a clock edge. The characteristic equation for the flip-flop is obtained from the circuit.

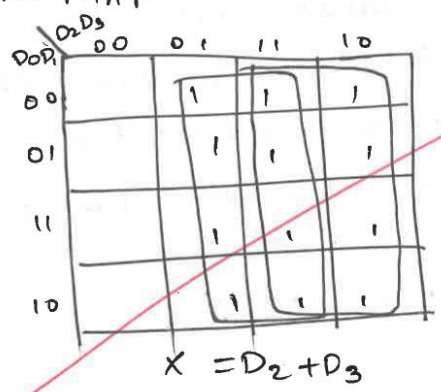
$$Q(t+1) = T \oplus Q = TQ' + T'Q$$

7) What is priority encoder design 4 to 2 line priority encode with diagram.

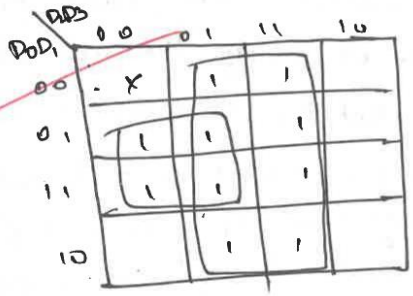
→ A priority encode is an encode circuit total includes the priority function, and handels the possibility that input might be in contention.

Inputs				Outputs		
D_0	D_1	D_2	D_3	X	Y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

K- MAP

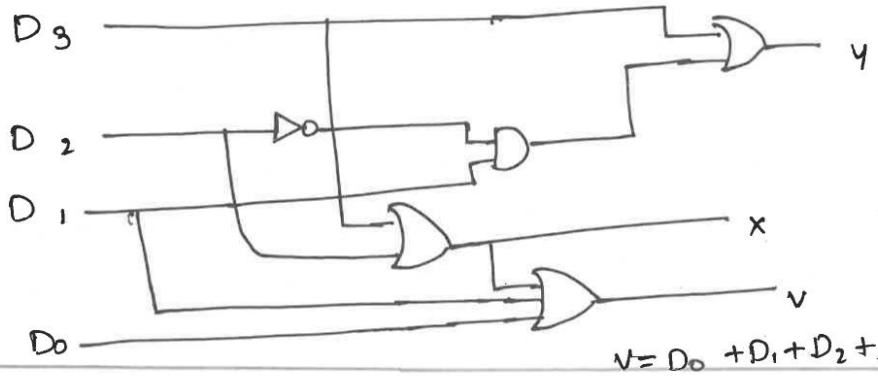


$X = D_2 + D_3$



$X = D_3 + D_1 D_2'$

Circuit diagram



$V = D_0 + D_1 + D_2 + D_3$

8) Design and Explain 4 bit adder with carry look ahead.

→ The construction of a four-bit adder with a carry look ahead each sum output requires two exclusion-OR gate.

The output of the first esculusion-OR gate generate Pi variable and the AND Gate generate the G_i variable The carries are propogated through the carry look ahead generator and applied as inputs to the second Exclusive OR Gate All output carries are generate after a delay though only two level of gate. thus, output S_0 through S_3 have equal propogation delay times. the two-level circuitary for the output carry C_4 is not shown. This circuit can equaly be desired by the equation-substitution.

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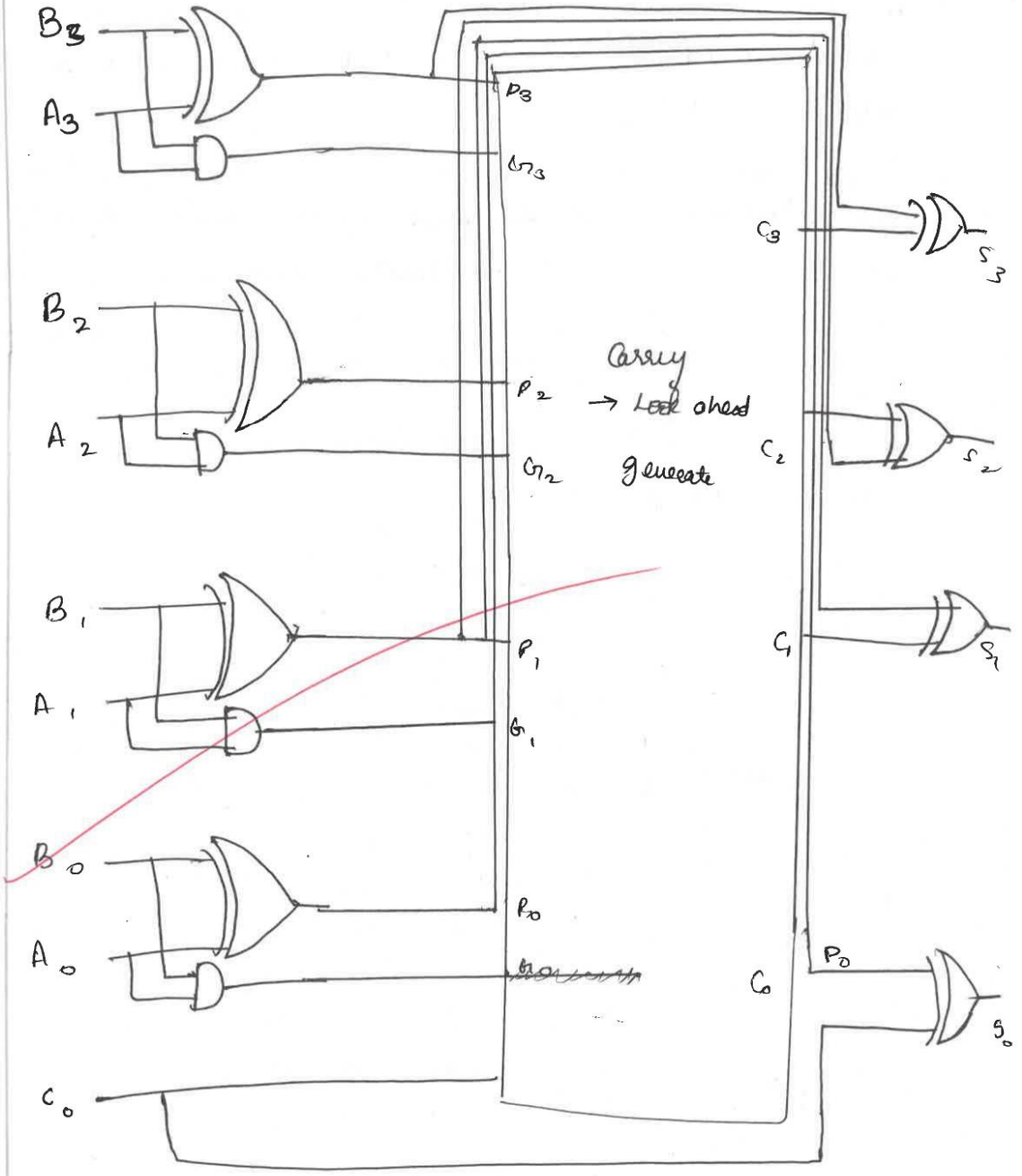
3)


B_3
A_3
P_3
G_3
C_3
S_3
B_2
A_2
P_2
G_2
Carry
→ Look ahead
generate
C_2
S_2
B_1
A_1
P_1
G_1
C_1
S_1
B_0
A_0
P_0
C_0
P_0
S_0
C_0

9) Design BCD to excess 3 code converter.

→ A code conversion is a circuit that makes the two systems compatable even though each uses a different binary code.

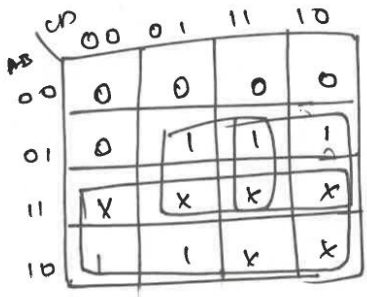
- Since each code uses four bits to represent a decimal digit. Hence there must be four input variables and four output variables, we designated the four input binary variables by the symbols A, B, C & D and the four output variables by w, x, y & z

- ADD 3 to BCD to get excess - 3 code.

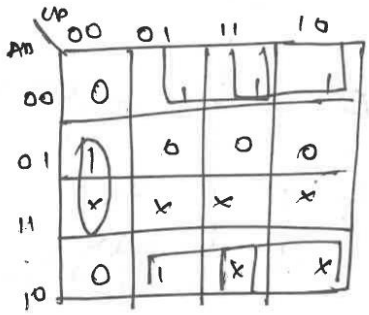
Truth Table.

Input BCD				Output excess-3 code.			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	0	1
1	0	0	1	1	1	0	0

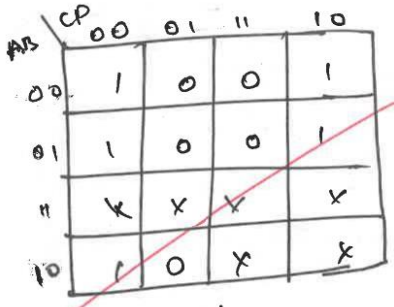
Note that four variables may have 16 bit combination but only 10 are insted in the truth table the six bit combination not listed for the input variables all dont care combination.



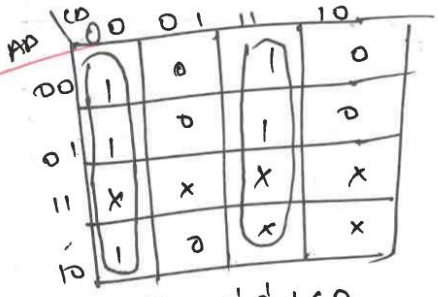
$W = A + BD + BC$



$X = B'D + B'C + BC'D'$



$Z = D'$



$y = C'D' + CD$

implemented with these or more level of gate

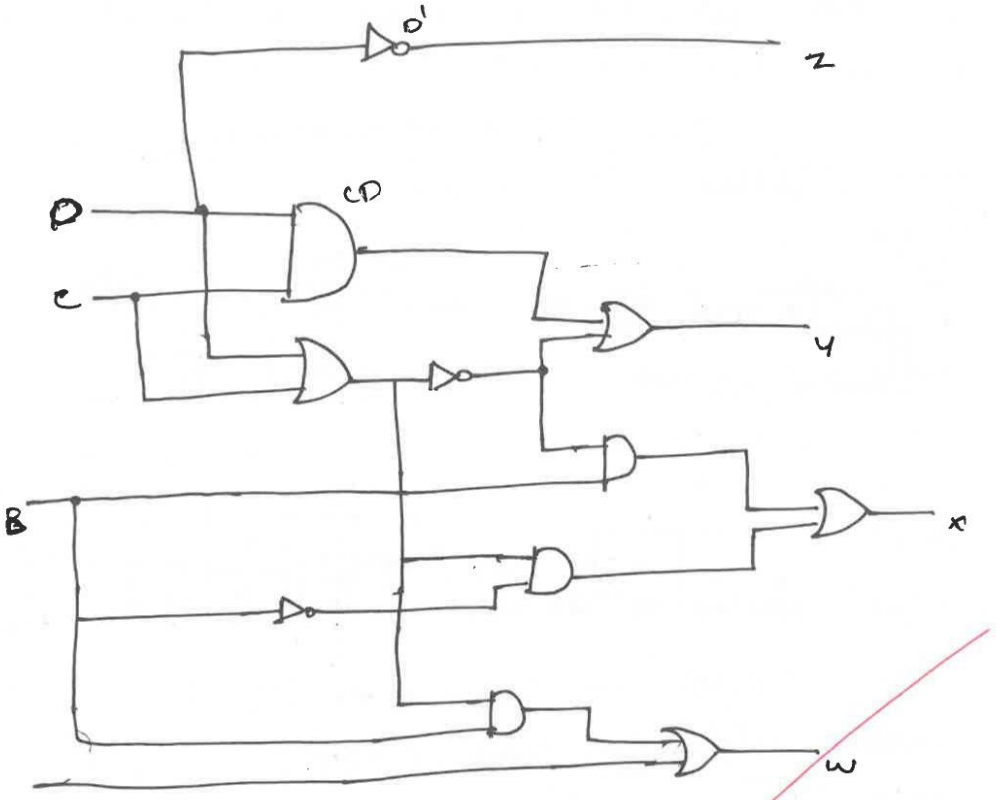
$Z = D'$

$y = CD + C'D' = CD + (C+D)'$

$X = B'C + B'D + DC'D = B'(C+D) + BC'C'$

$= B'(C+D) + B(C+D')$

$$W = A + BC + BD = A + B(C + D)$$



10) What is demultiplexer ? design 9:1 mux using 2:1 Mux

→ It is the process of separating a single input signal into multiple output signals. It is the opposite of multiplexing which combines multiple input signals into a single output signal.

Designing a 9:1 Mux using 2:1 Mux.

- A multiplexer is a circuit that selects one of several input signal & route it to a single output signal.

- To design a 9:1 mux using 2:1 mux - we can use hierchical append first design a 8:1 Mux using 2:1 Mux and then we use 3:1 mux to create a 9:1 Mux.

Step 1:- Design a 3:1 Muxing using 2:1 Mux

Mux 1 :- Select blw input A & B

Mux 2:- Selects blw the output of Mux 1 & Input

The control input for the 8:1 Mux all S_1 & S_2

S_1	S_0	output
0	0	A
0	1	B
1	0	C

step 2:- Design a 9:1 Mux using these 3:1 Mux.

Mux 1 : Selects blw inputs A, B & C

Mux 2: Selects blw inputs D, E & F

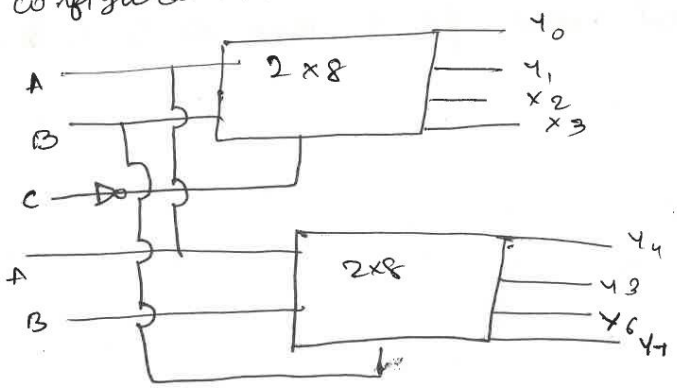
Mux 3: Selects blw inputs G, H, I

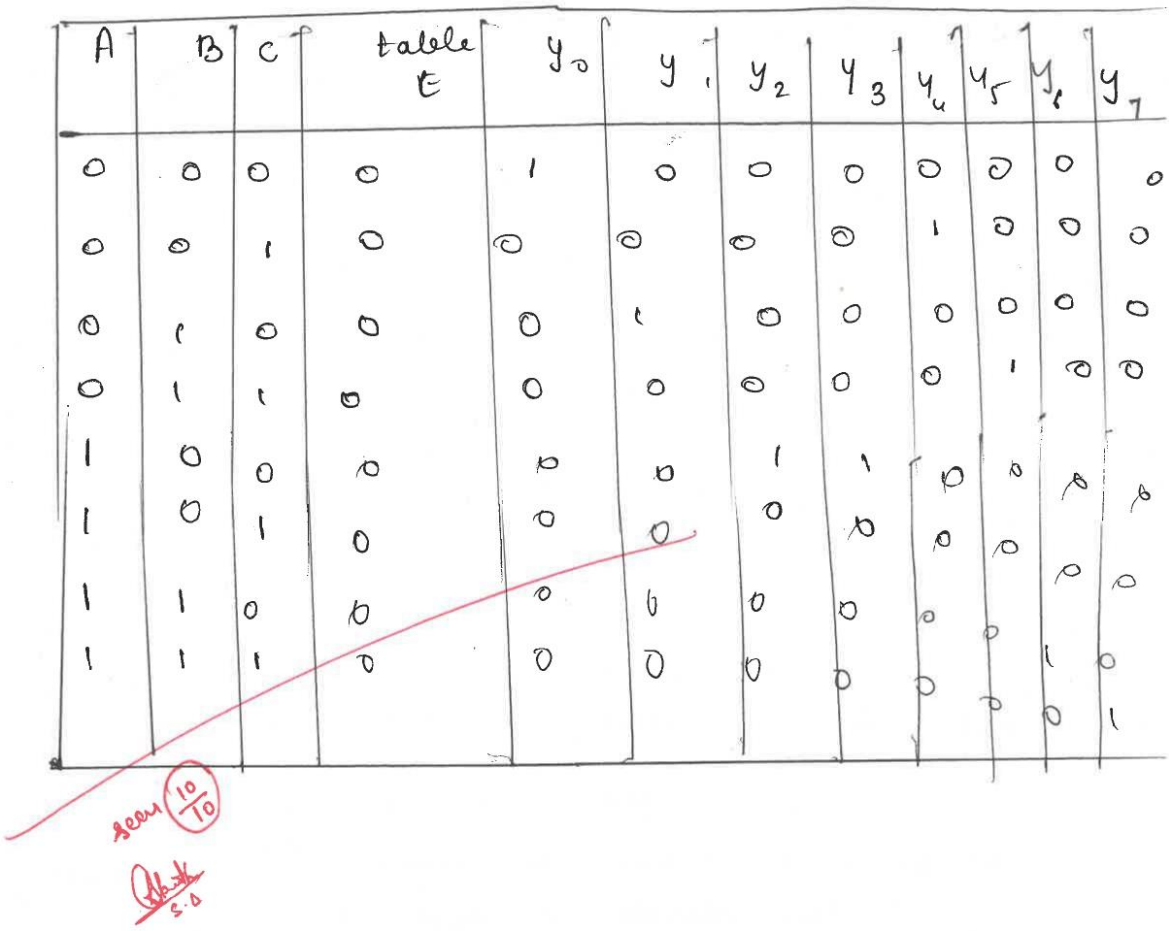
The control input for 9:1 Mux are S_2, S_1 & S_0.

S_2	S_1	S_0	Output
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H
-	-	-	I

Note that the output I is not used in this design.

Draw a logic diagram constructing 3 to 8 line decoder with active low enable using a pair of 2-4 line decode a truth table for the configuration.





A	B	C	table E	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0
0	1	0	0	0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	1	0
										0	1

score 10/10

S.D

Sample of Assignment Answer Booklet